Automatic Data Processing in the Wiring of a Digital Computer

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1, *Introduction*

In the development of today's computers, there is a large number of routine and manual repetitive desk works that must be performed; the drafting and checking of logic diagrams, the assignment of circuit components to a printed circuit card, of printed cards to frames; the wiring tabulation between the thousands of cards and so on. These tedious manual works should be performed by a digital computer. This paper describes some experiences gained by producing the automatic wiring tabulation of the ETL Mk-4B[1] under development, with using the ETL Mk-4A that has been constructed in our laboratory.

2. *Mechanization System of Data Processing in the Wiring*

The various phases of the mechanization system which were performed by authors are shown in Fig. 1. At the first phase, information on the original logic diagrams is transcribed on hole-sort-cards. Each hole-sort-card is assigned to each printed circuit card with 18 terminals. It contains the name of an amplifier with gates or of gates, their inputs which are also the names of the connected amplifiers, and the location of the assigned printed circuit card in the computer frames.

There are two types of standard printed circuit cards, the one is used for amplifiers with a small number of inputs and the other merely for complex gates. Because the basic circuitry of the ETL Mk-4B is of dynamic type, the same card is available for either an amplifier or a flip-flop. Although the hole-sort-cards used may be manually sorted by means of the punched holes, the sorting function is not necessarily essential in the following phases.

In the second phase, the items on the cards are recorded on a punched paper tape called the Master Tape. The M Tape is about 200 m long and thirty man-days of work is required for the key punching. The checking and correcting of the M Tape necessitate about one-third of the consumed time.

But some format errors of the M Tape are detected during the following machine runs and few errors which come from the misoperations of a puncher and a flexowriter still remain until the final phase.

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As the M Tape is the heart of the mechanization system, more nervous care should be paid to eliminate the causes of errors as possible.

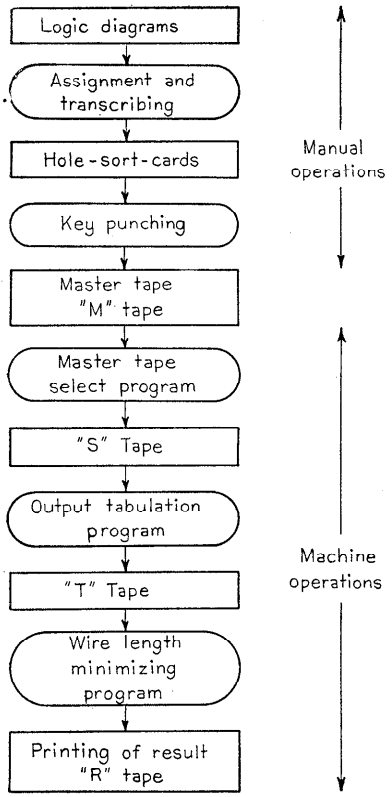

Fig. 1. Flow chart of the mechanization system for producing the wiring tabulation.

The S Tape is produced by extracting the names of cards and the corresponding locations from the M Tape. It takes the machine five hours.

The M Tape contains the complete records concerning the inputs. Collating the M Tape and the S Tape, all the outputs of each amplifier are searched and recorded on the T Tape. It takes ten hours. The machine time consumed at this phase and the foregoing phase is almost the operation time of the input-output machines. The net computation time is very short.

Information on the T Tape contains the output tabulation of each amplifier. But the output tabulation is not different from the required wiring tabulation, because the former indicates the optional ordering of output terminals depending on the M Tape.

From the T Tape the minimum wire length interconnected between output terminals of each amplifier is calculated. The programming and the consumed time at this phase is discribed in the next section. The resulted wiring tabulation is printed and copied as the R Tape.

3. *Programming*

The "master tape select program" and the "ouptut tabulation program" are very simple and therefore they are not described here. The most important one is the "wire length minimizing program".

If N numbers of terminals to be interconnected between them are given and the maximum number of branching from a terminal, C is not restricted, a rigorous solution for minimizing the total wire length is obtained.[2)]

The authors, however, employ C=2 from some technical reasons. In the case of C=2, the total wire length is in general longer than in the other cases. The wiring technique in turn takes advantage to make soldering and detecting of wiring errors easy.

Various methods are considered. One method used by authors is shown in Fig. 2. First, any terminal is selected as an initial point. A terminal which locates at the shortest distance from the first one is searched. In a similar fashion the process proceeds and a string of all terminals is obtained. Based upon this fundamental solution (first approximation), any two elements of the string are exchanged to reduce the path length connecting them. A number of times of the exchanging process is $N(N-1)/2$. From the process a minimum wiring length is eventually obtained. Altering the first initial point, the similar calculation is repeated $(N-1)$ times. A solution having the minimum total length out of the N solutions is the final solution.

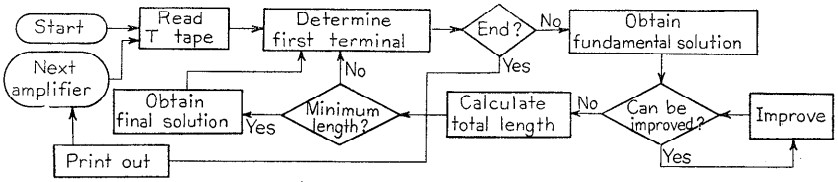

Fig. 2. Flow chart of "wire length minimizing program" (1)

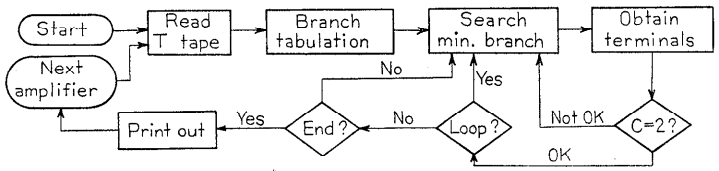

Fig. 3. Flow chart of "wire length minimizing program" (2)

Fig. 3 shows another method developed by authors. The length of all $N(N-1)/2$ branches is calculated. Firstly a branch of the minimum length is selected. If each terminal of the branch meets the condition: $C=2$, the other branches connecting the terminal are erased from the branch list. In the new branch list another branch of the minimum length is searched. The process is repeated until a complete string is produced. Note that a loop may be formed and the process must be terminated without getting a final solution.

The calculating time by means of these programs is propotional to N^3. The calculating time of the second program (Fig. 3) is shorter than that of the other one (Fig. 2) and it takes about $6.7 \times N^3$ ms. The total consumed time at this phase is about 50 hours.

4. *Summary*

Through the experiment described above an author's question is whether or not the mechanization system is economical. Most of the routine

work can be eliminated. But the programing effort is considerably tough and the program is not essential among computers. It is also evident that the keypunching operation is extremely time consuming.

It would be most significant that the complete record of the master tape can be available at other various design and maintenance stages; for example, a complete count of circuit components, the improvement of logic diagrams by logic simulation.

References

1. K. Fuchi and H. Nishino: System Design of ETL Mk-4B, An Input-Output Computer, in this issue pp. 66–69.
2. H. Loberman and A. Weinberger: Formal Procedures for Connecting Terminals with a Minimum Total Wire Length, Jr. ACM vol. 4 (1957) pp. 428–437.