RC-014

A Feasibility Study of Active Current Testing

Yukiya Miura †

Abstract

This paper proposes a new current testing method, active current testing, for detecting various fault classes of CMOS circuits. The proposed method is an extended method of VDD ramp testing, and it is carried out by applying various input signals for the circuit under test. If a power supply current is measured by changing both a power supply voltage and an input signal, we can make the internal condition of a circuit various. Then, fault detection by current testing becomes more effective than conventional VDD ramp testing.

We apply active current testing to two CMOS circuits, an operational amplifier and a level shifter, and demonstrate its fault detection ability. Except for the special case of circuit behavior, we found that active current testing can detect both hard faults (i.e., short and open faults) and soft faults (i.e., process variations and reliability degradation).

Keywords: *CMOS circuits, current testing, fault detection, input signal, ramp voltage*

1. Introduction

Current testing including IDDQ testing is well known as one of effective testing method for CMOS circuits; however, for deep submicron circuits, there was a negative and questionable opinion for using current measurement to detect faults in deep submicron circuits [1]. Nevertheless, it is still the effective method for circuit testing.

Process variations of deep submicron circuits cause a serious problem for circuit behaviors, identification between fault-free circuits and faulty circuits is difficult. Nowadays, CMOS technologies are widely used, for example, low voltage circuits, high frequency circuits (i.e., RF circuits), analog circuits, so on. Testing these circuits is becoming new research topics. Based on these backgrounds, application of current testing for identification of process variations and outlier screening [2]-[4], and fault detection of analog and RF circuits [5]-[7] have been studied.

S.S. Somayajula et. al. had proposed VDD ramp testing for RF circuits [8], [9]. The method is a kind of current testing by changing a power supply voltage. The basic idea of VDD ramp testing is that the change of circuit conditions causes several current signatures and that a faulty circuit shows different current signature compared with fault-free one when the VDD voltage is changed. The method showed good fault detection for hard faults of analog circuits. In addition, this method has the possibility for identifying circuit variations.

† Faculty of System Design, Tokyo Metropolitan University

A MOS transistor in a fault-free circuit operates in one of three regions: the saturation, the linear, or the cut-off regions. Utilizing the operation regions of MOS transistors can enable us to inform internal conditions and to model the behavior of a circuit consisting of MOS transistors. We call such a modeling method an operation-region (OR) model [10], [11]. Based on this model, we investigated the relationship between circuit behaviors and transistor's ORs and showed that the OR model can be used for circuit testing and diagnosis [12]-[14]. Our previous results showed that circuit variations and soft faults also cause the change in operation regions of MOS transistors.

The ramp voltage for the power terminal causes the change in operation regions. In addition this, if the input signal of the circuit is varied, the circuit also experiences several internal conditions. In this paper, we thus propose a now current testing method, ***active current testing***, that is carried out by changing both the supply voltage and the input signal. We show its feasibility and fault detection ability through circuit simulation. As target faults, this paper assumes the change in the transistor's threshold voltage as circuit variations and reliability degradation as well as short and open faults as hard faults. We evaluate the ability of active current testing by using the operational amplifier of ITC'97 benchmark circuits [15] and the level shifter.

The rest of the paper is organized as follows. Section 2 briefly introduces original VDD ramp testing. An active current testing method is presented in Section 3. Section 4 presents simulation results. We show the effectiveness of the proposed method through simulation results by using two CMOS circuits. Observations for simulation results are describes at Section 5. Finally, we conclude this work in Section 6.

2. Prior work (VDD ramp testing)

S.S. Somayajula et. al. had proposed VDD ramp testing that is a kind of current testing to monitor a power supply current flowing into a circuit under test (CUT) by changing a power supply voltage. Their method is motivated as follows.

The power supply current passing through the circuit, IDD, depends on both the circuit condition and the circuit topology. This relationship on the time domain is represented by

$$IDD(t)=f(O(t), T), \quad (1)$$

where O(t) is the operating condition of the circuit, and T is the circuit topology. The circuit condition, O(t), also depend on the power supply voltage, VDD(t). If either

O(t) or T of Eq. (1) is varied, IDD(t) is changed. When the ramp voltage is applied to the power supply terminal, transistors in the circuit experience several operation regions. A faulty circuit will show different O(t) and T compared with a fault-free circuit, and shows finally an abnormal current signature of IDD(t). The dotted area of Fig. 1(a) and Fig. 1(b) explains this idea. Therefore, VDD ramp voltage testing was proposed as an effective method for detecting faults of CMOS circuits including analog circuits.

Note that faulty IDD(t) will increase or decrease depending on a faulty circuit status, O(t) and T.

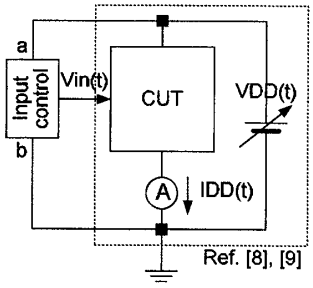

Fig. 1(a) Basic setup.

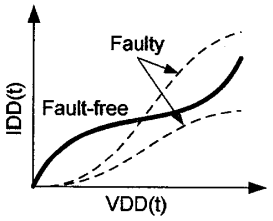

Fig. 1(b) IDD signature.

3. Active current testing

VDD ramp testing uses only the variable supply voltage for changing intentionally the internal condition of the circuit as follows [8], [9],

$$O(t)=g(VDD(t)). \quad (2)$$

In general, the circuit condition , O(t), also depends on an input signal; however, original VDD ramp testing did not mention the supply method of the input signal.

Our previous work, the OR model, showed that circuit conditions (i.e., operation regions of MOS transistors) depends on the input signal [10], [11]. So, Eq. (2) is represented by

$$O(t)=h(VDD(t), Vin(t)), \quad (3)$$

where Vin(t) is the input signal of the circuit. Therefore, we consider that the measurement of the power supply current, IDD, by changing both the power supply voltage and the input signal is further effective for detecting faults. We call this method ***active current testing***. Note that for secure circuit behavior, Vin(t)≤VDD(t) should be kept. Thus, we finally obtain

$$IDD(t)=f(VDD(t), Vin(t), T). \quad (4)$$

Figure 1(a) shows the basic setup for active current testing. In this setup, the input control circuit generates the input signal, Vin(t), so that Vin(t)≤VDD(t). Figure 2 shows examples of simple configurations of the input control circuit. The circuit of setup 1 generates a proportional voltage to VDD(t),

$$Vin(t)=(R2/(R1+R2))VDD(t). \quad (5)$$

On the other hand, setup 2 can generate an arbitrary input signal, Vin(t), when Vc(t) is controlled independently of VDD(t). Variable resistances R1, R2, and R3 should be prefixed before VDD(t) application. These resistances are realized by a biased MOS transistor as shown in Fig. 2(c).

As described the above, active current testing can set the CUT to various conditions, we consider that the abnormal current signature will appear easy if there is a fault or variation in the CUT.

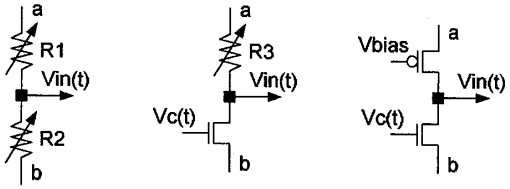

Fig. 2(a) Setup 1. Fig. 2(b) Setup 2a. Fig. 2(c) Setup 2b.

4. Simulation results

In order to verify effectiveness of active current testing, we use two CMOS circuits, operational amplifier (opamp) of ITC'97 benchmark circuit [15] and the level shifter (Fig. 3(a), and 3(b)). The level shifter is a special digital circuit and is difficult to test by a conventional testing method because the circuit functions as a complementary CMOS circuit and bridging faults at specific locations cannot be detected by logic testing and IDDQ testing, so we use this circuit. Technology parameters used by circuit simulation are MITEL 1.2-μm for the opamp and TSMC 0.18-μm for the level shifter.

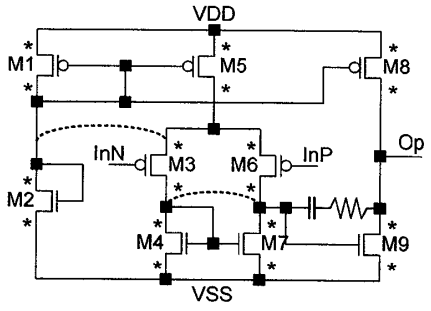

Fig. 3(a) Operational amplifier (opamp).

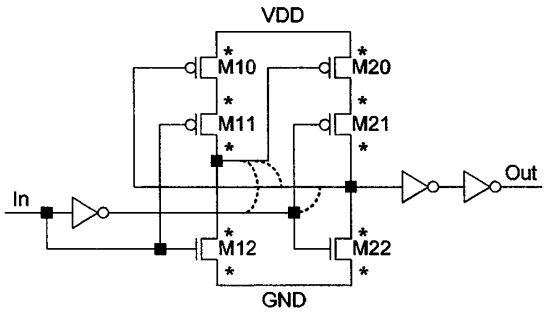

Fig. 3(b) Level shifter.

Table 1 Simulation conditions.

	Opamp	Level shifter
Technology	MITEL 1.2μm (ITC'97)	TSMC 0.18μm
VDD, VSS	+5V, -5V	+4V, 0V (GND)
Ramp VDD	-5V –> 5V	0V –> +4V
IDD	measurement@0.5V-step	measurement@0.5V-step
Vin (setup 1)	{(1/3), (1/2), (2/3)}VDD	{(1/3), (1/2), (2/3)}VDD
# Trs.	9	6
# Open faults	18@1GΩ	10@1GΩ
# Short faults	11@{1Ω, 1kΩ, 1MΩ}	9@{1Ω, 1kΩ, 1MΩ}
# Vt shift faults	9@{+30%, -30%}	6@{+30%, -30%}
# Total faults	69	49

Table 1 summarizes simulation conditions. Hard faults of two types, open faults and short faults, are assumed. Short faults modeled by resistances listed in Table1 are inserted between source and drain terminals of MOS transistors and between internal signal lines as shown by dotted lines in Figs 3(a) and 3(b). Locations of short faults between signal lines are randomly selected because we do not have layout information. Open faults modeled by 1GΩ resistance are inserted respectively to source and drain terminals of MOS transistors as shown by "*" marks. On the other hand, process variations become the important issue for testing deep submicron circuits and analog circuits. In addition, reliability degradation such as negative bias temperature instability (NBTI) and channel hot carrier (CHC) has the impact for nanoscale transistors [16]. For these problems, we also assume the shift of the transistor threshold voltage, Vt shift faults. IDD measurement is carried out by every 0.5-V step for ramp VDD. Input voltage is applied by the setup 1 configuration of Fig. 2(a).

Figures 4(a) and 4(b) show IDD signatures of the fault-free opamp and the fault-free level shifter, respectively. IDD signatures of 20k/10k ((1/3)VDD) and 10k/10k ((1/2)VDD) for the opamp are the quite same. As shown these figures, the IDD signature depends on both VDD and input signals. Note that IDD value of the faulty circuit is increased and decreased than that of the fault-free circuit, which depends on fault types, VDD vaults, and input signals. Then, we evaluate the fault IDD signature by using absolute values of the different voltage. Fault detection is carried out by comparing IDD values of Figs. 4(a) and 4(b) with those of CUTs of every 0.5-V step of the ramp voltage.

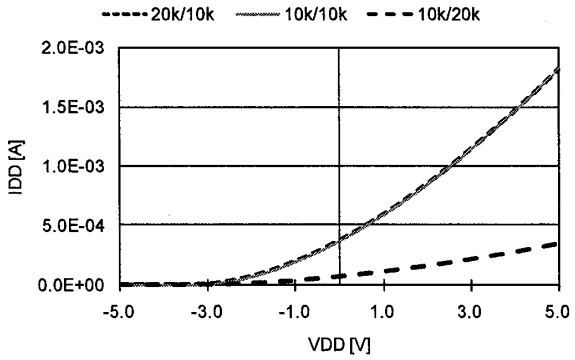

Fig. 4(a) IDD signature of fault-free opamp.

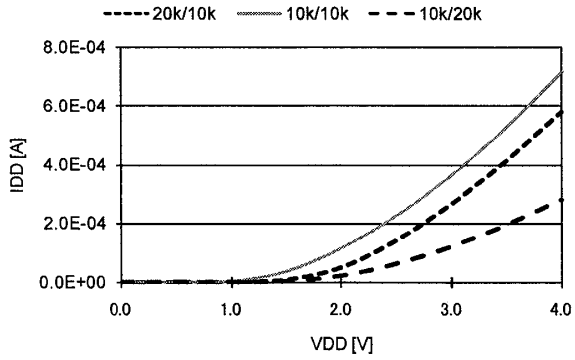

Fig. 4(b) IDD signature of fault-free level shifter.

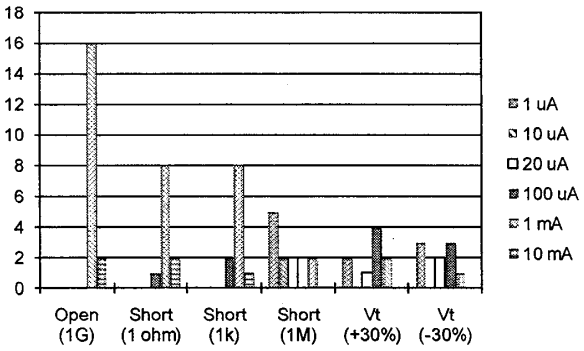

Fig. 5(a) Distribution of IDD difference of opamp.

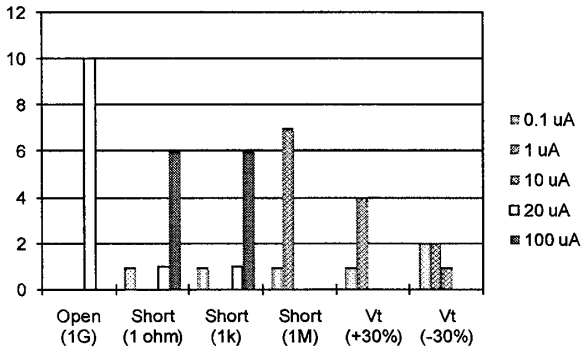

Fig. 5(b) Distribution of IDD difference of level shifter.

Table 2 Summary of fault detection

		Opamp				Level shifter			
		20k/10k	10k/10k	10k/20k	proposed	20k/10k	10k/10k	10k/20k	proposed
Open		100.0%	66.7%	100.0%	100.0%	100.0%	30.0%	70.0%	100.0%
Short	(1Ω)	90.9%	81.8%	90.9%	100.0%	77.8%	66.7%	66.7%	98.1%
	(1kΩ)	90.9%	81.8%	90.9%	100.0%	77.8%	66.7%	66.7%	98.1%
	(1MΩ)	72.7%	54.5%	81.8%	100.0%	77.8%	44.4%	55.6%	98.1%
Vt shift	(+30%)	77.8%	44.4%	100.0%	100.0%	66.7%	0.0%	16.7%	83.3%
	(-30%)	77.8%	55.6%	100.0%	100.0%	66.7%	0.0%	16.7%	83.3%
Total		87.0%	65.2%	94.2%	100.0%	79.6%	38.8%	53.1%	91.2%

Figure 5(a) and 5(b) show distributions of the absolute difference of IDD values between the fault-free and faulty circuits of the opamp and the level shifter, respectively. Faulty opamps generate at least 1 μA difference compared with the faulty-free opamp, and all the faults are detected by the proposed method. On this other hand, the faulty level shifter generates at least 0.1 μA difference, and we assume that this different current is measurable. Except for the short fault and the Vt shift fault of a specific one transistor, M20, the other faults are detectable.

Table 2 shows comparison of fault detection between conventional ramp testing and proposed active current testing. Conventional ramp testing used one of three input signals (i.e., fixed input signal), the highest fault detection ratios of the opamp and the level shifter are 94.2% and 79.6%, respectively. The proposed method used the all of three kinds of input signals, and detection ratios of those CUTs increased to 100% and 91.2%, respectively. In this simulation, we assume to use three input signals for all faults. If a suitable input signal considering the CUT type and the fault type can be applied to the CUT, active current testing is further effective.

From these results, we can say that active current testing is effective for detecting hard faults and soft faults of CMOS circuits. Especially for analog circuits, the proposed method is more effective than original VDD ramp testing. However, application of active current testing to static CMOS logic circuits may be difficult because the input signal becomes like a square wave signal (i.e., logic values) as the number of logic gate stages increases.

5. Observations

(1) In general, it is said that current testing or IDDQ testing is effective for detecting short faults. However, open faults also generate IDD change. This is because that node voltages between VDD and GND (or VSS) are changed by the open fault (i.e., the large resistance in the VDD-GND path), and this causes the change in the internal condition of the CUT (i.e., operation regions of MOS transistors). Finally, IDD changes and active current testing can detect open faults.

(2) Vt shift faults cause the relatively large change in IDD current. This is because that transistor's operation region is changed by the fault, and this change becomes noticeable by active current testing. From our previous works, circuit variations and parameter changes influence to operation regions of MOS transistors [13]. In this sense, active current testing is effective for detecting this kind of faults.

(3) A specific transistor of the level shifter is not testable, that is M20 of Fig. 3(a). Short faults and Vt shift faults of M20 are not detected. This is explains as follows. Figure 6 shows operation regions of M20, M21, and M22 of the fault-free level shifter when Vin and VDD are changed. M21 and/or M22 are the cut-off or saturation regions, and the current path from VDD to GND is not formed even if there is the fault. Therefore, IDD never flows into this path formed by M20, M21, and M22, and faults of M20 are not detected. However, open faults of M20 is detectable because these faults cause the node voltage change around M20 and operation conditions of M21 and M22 are changed, then IDD change occurs.

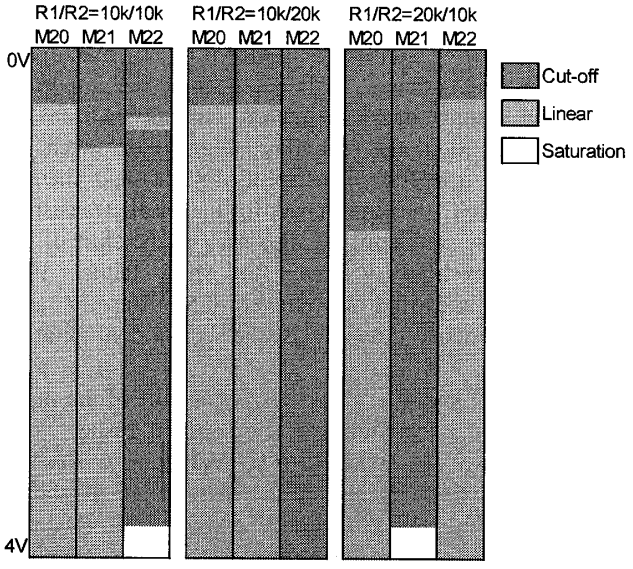

Fig. 6 Operation regions of level shifter.

(4) Active current testing uses several input signals. Figure 7 shows IDD signatures of several faults of the opamp. Even if one fault is considered, the IDD signature

is varied by the input signals. Therefore, current measurement by changing the input signal is effective. Note that IDD signature is not a linear function, it depends on fault types and input signals.

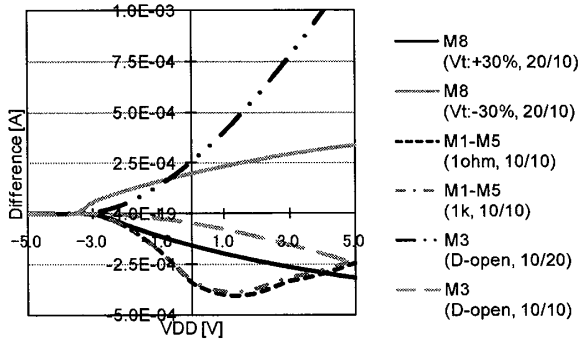

Fig. 7 IDD signatures.

(5) Discussions until here assume that active current testing is used for the stand alone circuit. Application of active current testing to the embedded CUT is proposed. The circuit of Fig. 8 shows the setup for the embedded CUT (setup 3) and is called ***embedded active current testing***. In this setup, one pull-down nMOS transistor, Md, is added, and the logical value 0 is applied to the gate G which is the gate to drive the node N (i.e., pMOS transistor Mp of G is the on-state and acts as a load). This configuration forms the pseudo nMOS logic circuit, the input signal of the embedded CUT, Vin(t) (i.e., the output voltage of the pseudo nMOS logic), is generated by the gate control signal, Vc(t). The range of Vin is given by

$$V_{OH} = VDD, \tag{6}$$

$$V_{OL} = (VDD - V_t)(1 - \sqrt{1 - \frac{\beta_p}{\beta_n}}), \quad V_t = V_{tn} = |V_{tp}|, \tag{7}$$

where βp and βn represent MOS transistor gain factors of Mp and Md, respectively [17]. For simple discussion, although we assume the gate G is a NOT gate, this method can be applied to other gate types.

Embedded active current testing is applicable for CMOS circuits because the node N is connected to gate terminals of the embedded CUT. Note that for the implementation of embedded active current testing, the power terminal of the embedded CUT needs to separate from other circuits.

Figure 9 shows the implementation example for the level shifter, where transistor sizes of Mp and Md are shown. Figure 10 shows simulation results of the circuit of Fig. 9 when several input signals are used. Setup 1 is the our original method described in Sect. 4, while setup 3-1 and setup 3-2 are results by using the gate control signal, Vc(t), as embedded active current testing. For setup 3-1, Vc(t)=VDD(t), while for setup 3-2, Vc(t) is an independent variable DC voltage. By using setup 3-2, we can generate a complex and arbitrary input signal for the CUT, and finally the arbitrary IDD signature appears. Therefore, we expect that active current testing such as setup 2 and setup 3 is more effective for circuit testing.

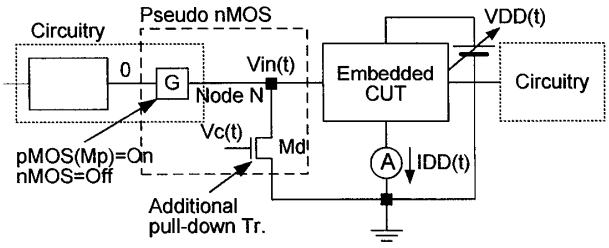

Fig. 8 Embedded active current testing (setup 3).

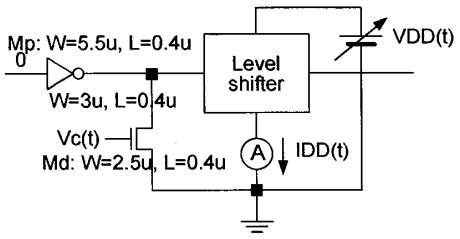

Fig. 9 Setup for level shifter (setup 3).

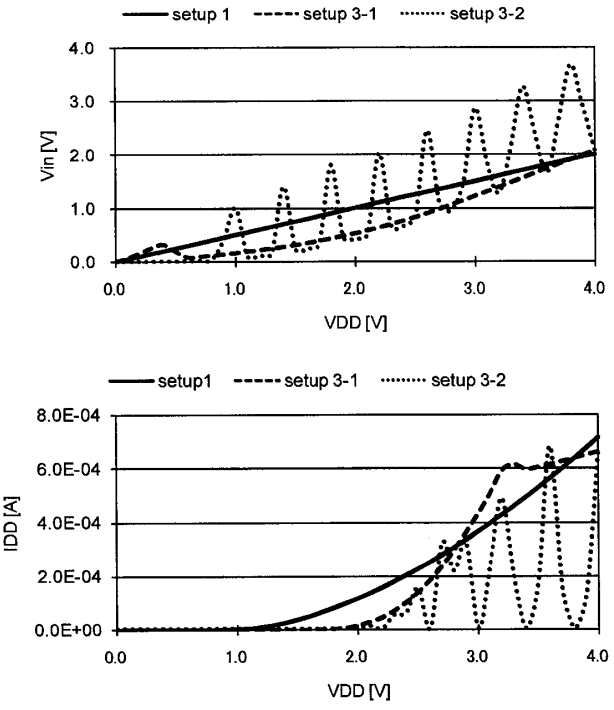

Fig. 10 IDD signature of independent Vin.

6. Conclusions

This paper proposed active current testing by changing both the supply voltage and the input signal. Especially controlling the input signal, we could produce various internal conditions of the CUT intentionally. We also proposed several setups for implementing active current testing. Except for the special case of the circuit condition, all of the hard faults and Vt shift faults are detected by the proposed method. In this case study, we consider that active current testing is effective for detecting hard and soft faults including process variations and reliability concerns. For future works, we need to verify the test ability of active current testing by using several circuit types and fault types including process variation and reliability degradation, the effective application method of the power supply and the input signal, and evaluation of a testing cost.

Acknowledgement

This work was partially supported by JST, CREST.

References

[1] J.M. Soden and C.F. Hawkins, "IDDQ Testing: Issues Present and Future," IEEE Design & Test of Computers, vol.13 , no.4, pp.61-65, December 1996.

[2] P. Nigh and A. Gattiker, "Random and Systematic Defect analysis Using IDDQ Signature Analysis for Understanding Fails and Guiding Test Decisions," Proc. Int. Test Conf, pp.309-318, 2004.

[3] B. Turakhia, B. Benware, R. Madge, T. Shannon, and R. Daasch, "Defect Screening Using Independent Component Analysis on IDDQ," Proc. VLSI Test Symp., pp.427-432, 2005.

[4] S.S. Sabade and D.M. Walker, "IC Outlier Identification Using Multiple Test Metrics," IEEE Design & Test of Comput., vol.22, no.6, pp.586-595, Nov.-Dec. 2005.

[5] A. Gopalan, M. Margala, and P.R. Mukund, "A Current Based Self-test Methodology for RF Front-end Circuits," Microelectronics Journal, vol. 36, no.12, pp.1091-1102, Dec. 2005.

[6] S.S Akbay, S. Sen, and A. Chatterjee, "Testing RF Components with Supply Current Signatures," Proc. Asian Test Symp., pp.393-398, 2007.

[7] M. Cimino, H. Lapuyade, M. De Matos, T. Taris, Y. Deval, and J.B. Bégueret, "A Bobust 130nm-CMOS Built-In Current Sensor Dedicated to RF Applications," Journal of Electronic Testing: Theory and Applications, vol. 23, no. 6, pp.593-603, 2007.

[8] S.S. Somayajula, E. Sánchez-Sinencio, and J. Pineda de Gyvez, "Analog Fault Diagnosis Based on Ramping Power Supply Current Signature Clusters," IEEE Trans. Circuits and Systems-II: Analog and Digital Signal Processing, vol. 43, no.10, pp.703-712, Oct. 1996.

[9] J. Pineda de Gyvez, G. Gronthoud, and R. Amine, "VDD Ramp Testing for RF circuits," Proc. Int. Test Conf., pp.651-658, 2003.

[10] Y. Miura, "Fault Behavior and Change in Internal Condition of Mixed-Signal Circuits," IEICE Trans. Inf. & Syst., vol.E83-D, no. 4, pp.943-945, April 2000.

[11] Y. Miura, "A Novel Approach for Modeling Behavior of Analog and Mixed-Signal Circuits Based on an Operation-Region Model," Proc. European Test Workshop 2002, pp.215-217, 2002.

[12] Y. Miura and D. Kato, "Analysis and Testing of Analog and Mixed-Signal Circuits by an Operation-Region Model: A Case Study of Application and Implementation," Proc. 18th IEEE Int. Symp. Defect and Fault Tolerance in VLSI Systems, pp.279-286, 2003.

[13] Y. Miura and J. Kato, "Adaptive Fault Diagnosis of Analog Circuits by Operation-Region Model and X-Z Zoning Method," Journal of Electronic Testing: Theory and Applications, vol.24, no.1-3, pp.223-233, June 2008.

[14] Y. Miura and J. Kato, "Diagnosis of Analog Circuits by Using Multiple Transistors and Data Samplings," Proc. 23rd IEEE Int. Symp. Defect and Fault Tolerance in VLSI Systems Symposium, pp.491-499, 2008.

[15] B. Kaminska, K. Arabi, I. Bell, P. Goteti, J.L. Huertas, B. Kim, A. Rueda and M. Soma, "Analog and Mixed-Signal Benchmark Circuits - First Release," Proc. Int. Test Conf., pp.183-190, 1997.

[16] W. Wang, V. Reddy, A.T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, "Compact Modeling and Simulation of Circuit Reliability for 65-nm CMOS Technology," IEEE Trans. Device and Materials Reliability, vol.7, no.4, pp.509-517, December 2007.

[17] J.M. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall, NJ, 1996.