RC-011

A Case Study on Identification of Circuit Variation by Transistor States

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1. Introduction

Nowadays, the problem of circuit variation for deep submicron technologies is a serious issue in circuit design and testing areas. Especially, process variations directly affect to yield and reliability of products [1], [2]. As the elimination of process variations is difficult, design techniques such as design for manufacturing, design for yield and design for reliability, and statistical approaches for testing are used [3]-[5]. For detection and identification of process variations, observations of several parameters and multiple threshold levels are effective [5].

Countermeasures for process variations of digital circuits are well studied; however, countermeasures for analog circuits are not so much. Since analog circuits are widely used in SoCs and mobile electronic equipments, we need to investigate countermeasures for process variations of analog circuits. In addition, it is said that analog circuits are the fault tolerance circuit by their nature [6]. In this sense, identification of error tolerance (i.e., circuits with process variations) of analog circuits is difficult.

In this paper, we propose a new method for identifying circuit variation from a new aspect. We are proposing the operation-region (OR) model that can model/analyze circuit behavior by using transistors' operation regions [7]-[9]. Since the OR model utilizes the change in operation regions of transistors, it is possible that the OR model can detect variations of circuit behaviors by the change of transistors' operation regions. In this paper, we examine the effectiveness of the OR model for identifying the circuit with process variations. As the first step of this study, we consider only the variation in capacitance and resistance of an analog circuit.

Section 2 describes the basic idea for identifying circuit variation. Section 3 shows simulation results by using ITC benchmark circuits. In Section 4, we conclude this study.

2. Identification of circuits with variations

2.1 Operation-region model

A MOS transistor in a fault-free circuit operates in one of three regions: the saturation (S), the linear (L), or the cut-off region (C). The operation regions of some transistors in a circuit change to other regions when any input is applied to the circuit or if there is any variation in the circuit. Utilizing the operation regions of MOS transistors can enable us to model the behavior of a circuit consisting of these transistors. We call such a modeling method an *operation-region model* (*OR model* for short) (Fig. 1). For generating the OR model, (1) apply input signals to the CUT, (2) sample node voltages, Vd, Vg, Vs, of each transistor, and (3) calculate ORs of each transistor. A transistor's OR arranged in time series is called an *OR sequence*, which consists of OR data and time data. The length of the OR sequence is called *OR length* (see Fig. 1). Since the OR model can represent circuit behavior by discrete data, it has features of easy handling of the model and easy data processing.

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Based on this model, we investigated the relationship between circuit behaviors and transistor's ORs and showed that the OR model can be applied to circuit testing [7]-[9]. We found that when circuit behavior changes from fault-free status, the ORs of transistors in the circuit also change from fault-free status, and vice versa. Note that the OR of a transistor in a faulty circuit may become another operation region (O) which does not belong to any in three regions; e.g., if a reverse voltage is applied to a transistor terminal due to a bridging fault between the terminal and another signal line, the transistor's OR is calculated as "O". As a result, we must consider four ORs for the OR model for modeling circuit behavior. It is generally difficult to observe the ORs of transistors in a real chip. However, since circuit simulation is usually carried out at the design phase, we assume to use simulation data for generating the OR model in this research.

From our previous results, we found the following relationship [7], [8].

(a) If the influence of a fault on circuit behavior is large, the change in operation regions is also large.

(b) If the influence of a fault on circuit behavior is small, the change in operation regions is also small.

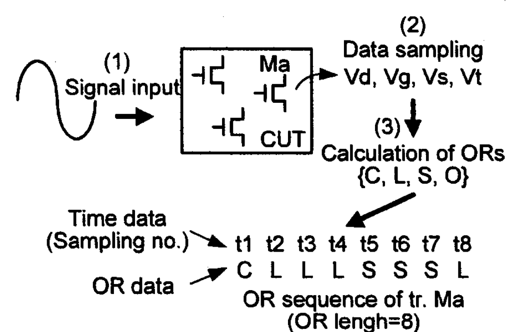

Fig. 1. Operation-region model.

As the example of the above relationship, Fig. 2 depicts the distribution of OR change of a circuit (i.e., the CT filter of Section 3), where the x-axis shows the circuit number that is arranged in order of variation of +6σ, .. , +1σ, -1σ, .. , -6σ (|1σ| step) for each element and the y-axis shows the count of different OR data in the OR sequence between the typical circuit (i.e., golden circuit) and the variation circuit. Terminologies in the figure are explained in the Sect. 2.2. Circuits with |6σ| variation (i.e., the crest

of the wave form graph) give a large value of OR change. On the other hand, circuits with |1σ| variation (i.e., the trough of the wave form graph) give a small value. Therefore, we can say that the change in OR sequence reflects the magnitude of circuit variation. Thus, the use of transistors' OR is reasonable for evaluating circuit variation and circuit behavior.

Note that in this paper, we assume that transistor states (transistors' operation region) are observable or the proposed method is carried out by using circuit simulation.

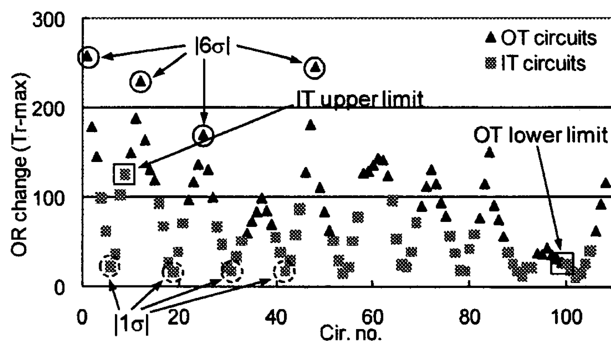

Fig. 2. Distribution of OR change.

2.2 Analysis method

This study is motivated by the fact that the change in operation regions of MOS transistors has the relation with circuit conditions (i.e., circuit behaviors). In order to investigate the relationship between circuit variation and influence on operation region change, we use the following method.

(1) Give circuits with resistance and capacitance variations from ±1σ to ±6σ. In this paper, we only consider variations of the resistance and the capacitance as the first step of this study. These circuits are classified into two types.

(a) The circuits having element variation with |3σ| or less: We call these circuits *inner tolerance circuits* (*IT circuits* for short).

(b) The circuits having element variation with |4σ| or more: We call these circuits *outer tolerance circuits* (*OT circuits* for short).

In this paper, we wish to identify that the IT circuit is fault-free and the OT circuit is faulty, because we consider that variations within |3σ| are in error tolerance. Thus, we classify circuits into two sets, IT circuits and OT circuits, and analyze circuits of each set for examining the relationship between circuit variation and OR change.

(2) Collect measurement values of observation items that are used for identification of circuit variation. From measured values, we extract limit values for identifying between IT circuits and OT circuits.

(3) Apply the limit values for circuits with variations from ±1σ to ±6σ and verify whether or not each circuit is identified to be fault-free or faulty.

If this identification for a circuit is not correct (i.e., The IT (OT) circuit is identified to be faulty (fault-free).), we identify that the circuit is unknown (i.e., The circuit is neither fault-free nor faulty.).

Figure 3 depicts this approach. If we can find the maximum value for inner tolerance circuits when a certain item is measured, the circuit with a value more than the maximum value is judged as faulty. Conversely, if we can find the minimum value for outer tolerance circuits when a certain item is measured, the circuit with a value below the minimum value is judged as fault-free. Note that we call a limit value for identifying the fault-free circuit an *OT lower limit* (corresponding to the minimum value of OT circuits) and a limit value for identifying the faulty circuit an *IT upper limit* (corresponding to the maximum value of IT circuits). Figure 2 is the example of the distribution of measurement values and two limits of an actual circuit.

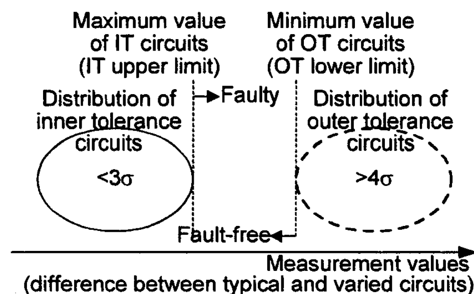

Fig. 3. Faulty circuits vs. fault-free circuits.

2.3 Objectives

Generally distribution of circuit variations is complex. Figure 4 shows a general model of circuit distribution that we consider in this paper. In this model, there is an overlap of the distribution between IT circuits and OT circuits. We can divide this distribution into three parts.

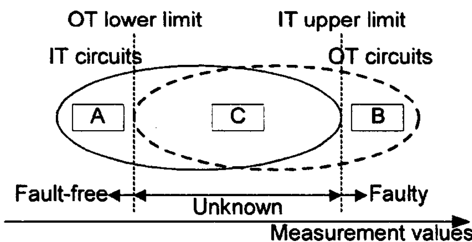

Fig. 4. Limit setting for variation identification.

Area A: These variation circuits have values of inner tolerance. We can identify that circuits are surely fault-free for IT circuits.

Area B: These variation circuits have values of outer tolerance. We can identify that circuits are surely faulty for OT circuits.

Area C: Since some circuits have inner tolerance values and others have outer tolerance values, we cannot identify whether circuits are faulty-free or faulty. We identify that these circuits are unknown.

Objectives of this paper are as follows.

(1) How do we draw the OT lower limit and the IT upper limit?

(2) How do we minimize the unknown area?

(3) How do we process observed data that is used for identifying circuit variations?

3. Simulation results

3.1 Data processing

In this paper, we use two kinds of measurement items, circuit output voltage and transistor's operation-region (OR). For these items, we use the following data process methods for obtaining the OT lower limit and the IT upper limit. We call these data *measured data*. These processes are carried out for OT circuits and IT circuits, respectively.

(1) Output voltage

We measure the output voltage of each variation circuit and compare it with that of the typical circuit at each sampling time.

(1a) Max-diff: Maximum difference of the voltage between the typical circuit and the variation circuit

(1b) Sum-diff: Summation of the difference voltage between the typical circuit and the variation circuit

(2) OR change

We calculate the transistors' OR of each variation circuit and compare it with that of the typical circuit at each sampling time.

(2c) Total-OR: Summation of the number of change in OR sequences of all transistors

(2d) Tr-OR: Summation of the number of change in the OR sequence for each transistor

(2e) Tr-max: The maximum number of partial change in the OR sequence for each transistor

(2f) Tr-min: The minimum number of partial change in the OR sequence for each transistor

(2g) Tr-max2: The second maximum number of partial change in the OR sequence for each transistor

(2h) Tr-min2: The second minimum number of partial change in the OR sequence for each transistor

[Example] Considering results of Table 1, we obtain the following values that are used for either the OT lower limit or the OT upper limit. For the calculation of 2c, Table 1 assumes results of OR change observed by two different transistors.

Table 1. Example of OR sequence.

<table>
<tr><td>Sampling no.</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td></tr>
<tr><td>Typ. cir.</td><td>C</td><td>C</td><td>C</td><td>C</td><td>L</td><td>L</td><td>L</td><td>L</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>L</td></tr>
<tr><td>Var. cir.1 (Tr.1)</td><td>C</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>S</td><td>S</td><td>S</td><td>S</td><td>C</td><td>C</td><td>C</td><td>C</td><td>C</td></tr>
<tr><td>Partial change</td><td></td><td colspan="3">3</td><td></td><td colspan="2">2</td><td></td><td></td><td colspan="4">4</td><td>1</td></tr>
<tr><td>Var. cir.2 (Tr.2)</td><td>S</td><td>S</td><td>S</td><td>S</td><td>S</td><td>C</td><td>C</td><td>C</td><td>C</td><td>S</td><td>L</td><td>L</td><td>L</td><td>C</td><td>C</td></tr>
<tr><td>Partial change</td><td colspan="5">5</td><td colspan="4">4</td><td></td><td colspan="3">3</td><td colspan="2">2</td></tr>
</table>

(2c) 24, (2d) {10, 14}, (2e) {4, 5}, (2f) {1, 2}, (2g) {3, 4}, (2h) {2, 3} ¶

3.2 Results and observations

In this paper, we use two ITC'97 benchmark circuits, the continuous-time state-variable filter (CT filter for short) and the leap-frog filter (LF filter for short) that consist of 27 transistors and 54 transistors, respectively [10]. We give variation for resistance and capacitance whose values are obtained from [11]. We give variation for the individual resistor and capacitor and for all resistors and capacitors. Then, the numbers of variation circuits of the CT filter and the LF filter are 132 and 228, respectively. The numbers of IT circuits and OT circuits of two filters are equal.

Table 2 shows results of identification of circuit variation. The OT lower limit determines fault-free circuits among IT circuits (i.e., area A of Fig. 4). The IT upper limit determines faulty circuits among outer tolerance circuits (i.e., area B). Otherwise, a circuit is identified to be unknown (i.e., area C). At the part (a) in Table 2, the OT lower limit and the IT upper limit are obtained from all of the variation circuits. At the part (b) (i.e., C-limit) and the part (c) (i.e., R-limit), these limits are determined from circuits with capacitance variation and circuits with resistance variation, respectively. "Sub-total" and "Total" show the total number of identified circuits when a circuit is identified as fault-free/faulty by at least one limit data. From these results, we found the following.

(1) Accuracy of identification by output voltage (i.e., Max-diff and Sum-diff) was low.

(2) Accuracy of identification by change in ORs of all transistors (i.e., Total-OR) was also low.

(3) Accuracy of identification by change in ORs of each transistor (i.e., rows from Tr-OR to Tr-min2) was high. Especially, when C-limit and R-limit were used for identification, identification accuracy was high. This is considered that limit values are effectively extracted from measured values because they are determined from each kind of the variation element.

(4) If we used five kinds of measured data for limit setting (i.e., rows from Tr-OR to Tr-min2), we could identify fault-free/faulty circuits by the accuracy of 92% or more.

(5) Since most of unknown circuits were distributed around variations of $|3\sigma|$ and $|4\sigma|$, the proposed method could reasonably identify IT circuits and OT circuits. If we used all limits obtained from all measured data, only one variation circuit of the LF filter is an exception to this rule. We will elevate identification accuracy if we use other measured data for limit setting. Table 3 shows identification results of the CT filter, where hatched areas mean unknown circuits that are distributed around $|3\sigma|$ and $|4\sigma|$ (i.e., five circuits (7.6%) are unknown) .

(6) In Table 2, we used ORs of all transistors in circuits. If we select 7 transistors in the CT filter and 13 transistors in the LF filter for setting limit values of OR change, we can obtain the same identification accuracy as when we used all transistors.

Table 2. Simulation results.

	Circuit	CT filter				LF filter			
	Data	OT circuits (66 cirs.)		IT circuits (66 cirs.)		OT circuits (114 cirs.)		IT circuits (114 cirs.)	
		Faulty	Unknown	Fault-free	Unknown	Faulty	Unknown	Fault-free	Unknown
(a)	Max-diff	18.2%	81.8%	30.3%	69.7%	12.3%	87.7%	0.0%	100.0%
	Sum-diff	10.6%	89.4%	22.7%	77.3%	13.2%	86.8%	0.9%	99.1%
	Total-OR	10.6%	89.4%	45.5%	54.5%	20.2%	79.8%	1.8%	98.2%
	Tr-OR	37.9%	62.1%	57.6%	42.4%	53.5%	46.5%	21.9%	78.1%
	Tr-max	43.9%	56.1%	57.6%	42.4%	75.4%	24.6%	37.7%	62.3%
	Tr-min	60.6%	39.4%	12.1%	87.9%	67.5%	32.5%	10.5%	89.5%
	Tr-max2	56.1%	43.9%	12.1%	87.9%	77.2%	22.8%	48.2%	51.8%
	Tr-min2	59.1%	40.9%	39.4%	60.6%	77.2%	22.8%	41.2%	58.8%
	Sub-total	66.7%	33.3%	60.6%	39.4%	88.6%	11.4%	63.2%	36.8%
(b) C-limit	Tr-OR	39.4%	60.6%	90.9%	9.1%	66.7%	33.3%	13.2%	86.8%
	Tr-max	43.9%	56.1%	89.4%	10.6%	76.3%	23.7%	31.6%	68.4%
	Tr-min	60.6%	39.4%	87.9%	12.1%	87.7%	12.3%	14.9%	85.1%
	Tr-max2	68.2%	31.8%	100.0%	0.0%	86.8%	13.2%	50.9%	49.1%
	Tr-min2	62.1%	37.9%	95.5%	4.5%	82.5%	17.5%	47.4%	52.6%
	Sub-total	77.3%	22.7%	100.0%	0.0%	91.2%	8.8%	68.4%	31.6%
(c) R-limit	Tr-OR	57.6%	42.4%	60.6%	39.4%	57.0%	43.0%	86.0%	14.0%
	Tr-max	59.1%	40.9%	60.6%	39.4%	72.8%	27.2%	74.6%	25.4%
	Tr-min	60.6%	39.4%	87.9%	12.1%	70.2%	29.8%	0.0%	100.0%
	Tr-max2	83.3%	16.7%	98.5%	1.5%	78.1%	21.9%	64.9%	35.1%
	Tr-min2	69.7%	30.3%	40.9%	59.1%	76.3%	23.7%	53.5%	46.5%
	Sub-total	90.9%	9.1%	98.5%	1.5%	87.7%	12.3%	93.9%	6.1%
	Total	92.4%	7.6%	100.0%	0.0%	94.7%	5.3%	94.7%	5.3%

4. Conclusions

This paper proposed the identification method of circuit variation by using the output voltage and the transistor state. We applied the method to two filter circuits with variations of resistance and capacitance and verified its effectiveness. Identification accuracy by limit values based on the transistor state was higher than that by the output voltage. By using five kinds of measured data of the transistor state, we could identify fault-free/faulty circuits by the accuracy of 92% or more. In addition, most of circuits that we could not identify either fault-free or faulty were distributed around $|3\sigma|$ and $|4\sigma|$. Therefore, we could say that the proposed method had a reasonable ability for identification of circuit variation.

For the future works, we need to develop a method for setting limit values with higher accuracy for variation identification. We also need to apply the proposed method to circuits with variation of other circuit parameters.

Table 3. Identification results of CT filter.

	OT circuits			IT circuits						OT circuits		
	$+6\sigma$	$+5\sigma$	$+4\sigma$	$+3\sigma$	$+2\sigma$	$+1\sigma$	-1σ	-2σ	-3σ	-4σ	-5σ	-6σ
C1	1	2	3	4	5	6	7	8	9	10	11	12
C2	13	14	15	16	17	18	19	20	21	22	23	24
R1	25	26	27	28	29	30	31	32	33	34	35	36
R2	37	38	39	40	41	42	43	44	45	46	47	48
R3	49	50	51	52	53	54	55	56	57	58	59	60
R4	61	62	63	64	65	66	67	68	69	70	71	72
R5	73	74	75	76	77	78	79	80	81	82	83	84
R6	85	86	87	88	89	90	91	92	93	94	95	96
R7	97	98	99	100	101	102	103	104	105	106	107	108
all-C	109	110	111	112	113	114	115	116	117	118	119	120
all-R	121	122	123	124	125	126	127	128	129	130	131	132

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