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Open Fault Detection in CMOS Combinational Circuits by Logic Testing with Precharging

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1. Introduction

Nowadays, open faults become one of major defects because present VLSI design uses multiple metal layers and copper process technologies [1]-[3]. As the present deep-submicron VLSI operates under a low voltage supply and a high frequency, influence by open faults becomes noticeable and the circuit with the open fault shows various complicated fault behaviors.

Many methods for detecting open faults have been proposed [4]-[10]. Logic testing relies that an open fault location produces an error logic value when the fault is excited. However, internal conditions around the location depend on an applied test vector, and as a result, probability of fault detection as a logic error (i.e., the stuck-at fault) is low. Current testing to detect open faults (e.g., IDDT testing and IDD waveform measurement) uses an unstable internal condition in a logic circuit to cause a power supply current. In a logic circuit, since this unstable condition does not continue for a long time, the extraction of current variation is difficult. Moreover, application of current testing to a deep-submicron VLSI and a large circuit is questionable. Delay testing expects increment of a delay time when the fault is excited. However, it is difficult to estimate the delay time for the large circuit with various parameters and is a costly method.

Open faults are classified into two types: gate terminal open faults and source/drain terminal opens [8]. Gate terminal opens are often called floating gate faults or interconnect opens. Via opens and contact opens are included in those faults. Source/drain terminal opens are often called stuck-open faults. In this paper, we consider gate terminal open faults. Note that stuck-open faults can be detected by two-pattern test [11], [12].

In this paper, we first analyze electrical behaviors caused by the gate terminal open fault. Based on the analysis, we propose a new simple method for detecting open faults as logic error. In order to detect open faults by logic testing, we must assign a fixed logic value to an open fault location. To do this, we control a power supply voltage in DC domain. After we can set the logic value, we apply only one input vector to verify whether the circuit produces a correct output value or not.

In the following, Sect. 2 describes motivation and electrical behaviors of open faults. Section 3 shows a method for detecting open faults. Section 4 shows simulation results and a test plan. Section 5 concludes the paper.

2. Preliminary

2.1 Motivation

Consider the four-stage inverter chain circuit as shown in Fig. 1(a). There are three possible locations of gate terminal open faults between two inverters G2 and G3: f1, f2, and f3. The open fault of f1 makes gate terminals of both nMOS and pMOS transistors floating (i.e., the input line of the gate element is floating). We call this fault a gate-input open fault. The open fault of f2 or f3 results in the gate terminal open of either nMOS or pMOS transistors. We call this fault a transistor-input open fault. Here, based on the fault location, G2 is called a driving gate and G3 is called a driven gate.

In general, gate terminal open faults are modeled by a RC circuit as shown in Fig. 1(b) [13], [14], where Rf is an open resistance and Cw1 (Cw2) is a total wire capacitance between the signal line having an open fault and signal lines having the VDD (VSS) voltage. When the test vector t is applied to the logic circuit, Cw1 and Cw2 at the signal line i are calculated as

$$Cw1(t,i) = \sum_{line \in \{high\text{-}level\ voltage\}} Cw(line) \ , \quad (1)$$

$$Cw2(t,i) = \sum_{line \in \{low\text{-}level\ voltage\}} Cw(line) \ , \quad (2)$$

where Cw(line) denotes a wire capacitance between the signal line i and a signal line having the high-voltage/low-voltage. In this paper, we consider open faults inserting the fault model of Fig. 1(b) into f1 and f2 of Fig. 1(a). The open faults are moreover classified into two types: strong open faults (i.e., complete or high-resistance open) and weak open faults (i.e., resistive open) [2]. As the first step of this research, we mainly consider strong open faults in this paper.

In order to detect open faults by logic testing, it is necessary to assign an opposite value with an expected one to the fault location by a test vector. However, since voltages of signal lines around the fault location depend on an applied test vectors, values of Cw1 and Cw2 at the fault location also depend on the test vectors. This means that the node voltage of the fault location also depends on the test vectors. Therefore, the open fault cannot necessarily be certainly detected by traditional logic testing. Note that under a certain assumption, the voltage of the open fault node is in proportion to Cw1/(Cw1+Cw2).

The above difficultness concerned with open fault detection comes from voltage assignment at the fault location. If a known logic value can be compulsorily set to the fault location, fault detection by logic testing can be realized easily. In this paper, we propose a new logic testing with precharging which is realized by controlling the node voltage of the fault location. The method can detect open faults as a logic error.

2.2 Electrical behavior of open fault

In this section, for the sake of simple discussion, we consider the gate-input open fault f1 of Fig. 1(a). Figure 2(a) shows simulation results of the faulty circuit, where simulation conditions as follows: VDD=1.8V, Rf=100MΩ, Cw1=16fF, Cw2=8fF, (rising and falling times)=1nsec. Although the circuit has approximately 2μsec delay times, it functions normally. However, the voltage of the fault node N2 is unstable because

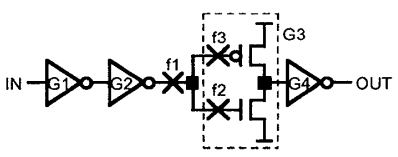

Fig. 1(a). Circuit model.

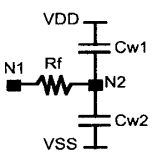

Fig. 1(b). Open fault model.

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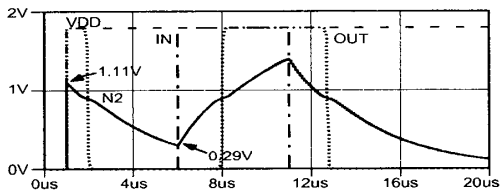

Fig. 2(a). Step voltage application.

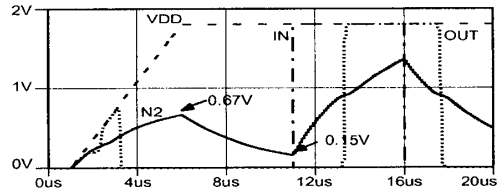

Fig. 2(b). Ramp voltage application.

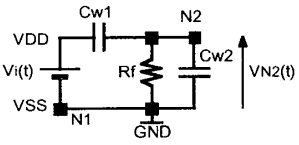

Fig. 3(a). Equivalent circuit of VDD application.

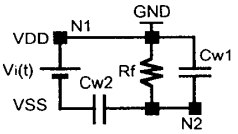

Fig. 3(b). Equivalent circuit of VSS application.

an intermediate voltage is generated. Especially, when the power supply voltage (VDD) is applied at 1μsec, the N2 voltage rises, and as a result, the circuit output becomes a high level even if the input value is a low level. On the other hand, if the power supply voltage is applied as the ramp voltage, the N2 voltage is relatively stable as shown in Fig. 2(b).

From these facts, if we control the power supply voltage in DC domain (i.e., application of the ramp voltage), we can assign a fixed voltage at the open fault location as an initial circuit condition. Moreover, if the voltage of the interconnect signal line are stable (i.e., the interconnect line is not switching for a time), the voltage at the open fault location is also stable. Here, voltages of the rectangular waveform are applied to each gate input because we cannot control rising and falling times of voltages of interconnect signal lines except for primary inputs.

In simulations of Figs. 2(a) and 2(b), voltages of all nodes are the GND level at time 0μsec, after that, the positive power supply voltage is applied to the VDD terminal. Therefore, the equivalent circuit with the fault f1 is represented by the RC differential circuit of Fig. 3(a) when N1=VSS=GND and VDD=(positive voltage). Here, if we apply the negative voltage to the VSS terminal (i.e., N1=VDD=GND, VSS=(negative voltage)), the equivalent circuit becomes one of Fig. 3(b).

In the RC differential circuit of Fig. 3(a), the voltage of the N2 node V_{N2} when the power supply voltage $V_i(t)$ is applied is expressed as follows:

$$V_{N2}(t) = \frac{Cw1}{Cw1 + Cw2} V_0 e^{-\frac{t}{Rf(Cw1 + Cw2)}}, \quad (3)$$

where $V_i(t)$=(step voltage) and $V_i(0)=V_0$.

$$V_{N2}(t) = k\,Cw1\,Rf\,(1 - e^{-\frac{t}{Rf(Cw1 + Cw2)}}), \quad (4)$$

where $V_i(t)=kt$ (ramp voltage) and $V_i(0)=0$.

Figure 4 shows simulation results of the circuit of Fig. 3(a), which agree with those of Figs. 2(a) and 2(b). Thus, this equivalent circuit is a reasonable model of the circuit with the open fault.

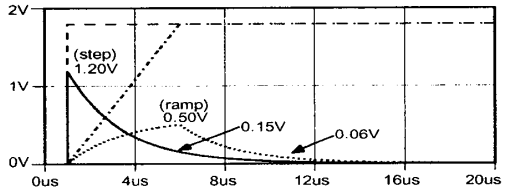

Fig. 4. Simulation results of Fig. 3(a).

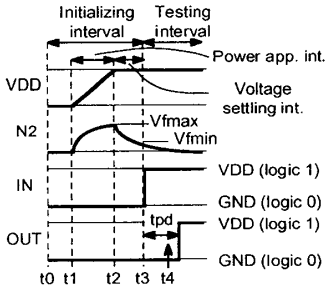

Fig. 5(a). Testing method for VDD application.

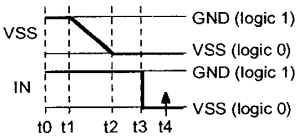

Fig. 5(b). Testing method for VSS application.

3. Principle of open fault detection

As described in Sect. 2.1, if we can surely assign a specific logic value to the fault location, it is very easy to apply logic testing for detecting open faults. Based on the fault behavior shown in Sect. 2.2, we propose the following method for assigning a specific voltage and detecting the fault by logic testing (Figs. 5(a) and 5(b)).

(1) First, all input terminals including power supply terminals of the circuit are set to the GND level at time 0 [t0]. In this case, all nodes in the circuit are set to the GND level.

(2) Second, a positive (negative) power supply voltage is applied to the VDD (VSS) terminal slowly (i.e., application of a ramp voltage) [t1, t2]. Note that since primary inputs are still the GND level, logic 0 (logic 1 for the negative VSS application) is still applied to the circuit. We call the interval [t1, t2] a power application interval.

(3) After the node voltage fully settles down [t3], apply one test vector to change a logic value of the open fault location and observe an output value at a predetermined time [t4]. We call the interval [t0, t3] an initializing interval. Moreover, we call the interval [t2, t3] a voltage settling interval.

(4) If the output value does not change within a specific time interval, we judge there is an open fault [t4]. Note that usually, the specific interval corresponds to one clock period of the at-speed of the circuit under test. We call the interval starting from [t3] a testing interval. In Fig. 5(a), this fault causes the delay time of tpd.

(5) The above procedure is repeated until every node predicted to be a fault location is checked.

Since the equivalent circuit with f1 is the circuit of Fig. 3(a) if we apply the positive power supply to the VDD terminal, the voltage of the fault node N2 is expressed by Eq. (4) for the power application interval and by Eq. (3) for the voltage settling interval. Note that since $V_{N2}(t)$ at t2 is given by Eq. (4), coefficient $(Cw1/(Cw1+Cw2))V_0$ of the right-hand side of Eq. (3) is given by $V_{N2}(t2)$ of Eq. (4). Here, the time constant τ of the differential circuits of Figs. 3(a) and 3(b) is $Rf(Cw1+Cw2)$.

Until here, we mainly consider to apply the positive power supply to the VDD terminal, where the initial logic value of the fault location is 0 and logic 1 is applied during the testing interval. If we apply the negative power supply voltage to the VSS terminal as shown in Fig. 5(b), the initial value is logic 1 and logic 0 for the testing interval.

According to Eq. (4), since the voltage of N2 is in proportion to both Cw1 Rf and Rf(Cw1+Cw2), we can estimate the voltage change of the fault location N2 as follows:

(1) Under t>Rf(Cw1+Cw2), the N2 voltage is in proportion to kCw1 Rf. If Cw1>Cw2, N2 voltage is easy to rise. Therefore, the application of the negative power supply to the VSS terminal is better for Cw1>Cw2. On the other hand, if Cw1<Cw2, N2 voltage is not easy to rise. Therefore, the positive power application to the VDD terminal is suitable.

(2) If the slope of the ramp voltage is constant, rising of the N2 voltage is easier as the time constant Rf(Cw1+Cw2) is larger. In order to prevent the voltage rising of N2, it is necessary to apply the ramp voltage of a gentle slope or to delay the application timing of a test vector.

4. Simulation results and test plan

To verify the proposed method, we carry out circuit simulation. Table 1 shows simulation conditions, where we use the TSMC 0.18μm technology [16]. Here, the wire capacitance of 8fF corresponds to the total wire capacitance between metal 6 of 20μm-length and 0.5μm-width and all other layers. We set an open resistance to 100MΩ anyway. The time constant is 100MΩ*88fF=8.8μsec for (Cw1, Cw2)=(80fF, 8fF). The table also shows timings of power supply and signal applications: t0 to t3 in Figs. 5(a) and 5(b). Since the ring oscillator frequency of 31-stage for 1.8V-VDD is 328.75MHz [16], we expect delay time of the fault-free circuit itself is smaller than 3nsec.

4.1 Simulation results for various parameters

4.1.1 Power supply application and wire capacitance

Table 2 shows the relationship between the voltage application type and the wire capacitance. Figures 6(a) and 6(b) show examples of simulation results of S1.

As described in the previous sections, the N2 voltage is proportional to Cw1 if the observation time is constant. Therefore, for the positive power supply application, when Cw1>Cw2 (i.e., large Cw1), the N2 voltage becomes higher, and the N2 voltage is lower for Cw1<Cw2 (i.e., small Cw1) (simulation no. S1). For the negative power supply application, the opposite phenomena occur because the equivalent circuit is denoted by the circuit of Fig. 3(b) (i.e., the role of Cw1 and Cw2 is exchanged) (simulation no. S2).

Since the time constant is Rf(Cw1+Cw2), tpd is small when (Cw1, Cw2)=(8fF, 8fF), however, for (Cw1, Cw2)={(80fF, 8fF), (8fF, 80fF)}, the delay time is almost the same.

From these facts, if Cw1<Cw2 (Cw1>Cw2), the positive (negative) power supply application is better. This means that the initial logic value 0 (1) is assigned to the fault location, and after that, logic 1 (0) is set by a test vector for detecting the fault.

The S3 simulation shows results of the equivalent RC circuit, where for (Cw1, Cw2)=(80fF, 8fF), the N2 voltage agrees approximately with simulation results of S1. For other values of (Cw1, Cw2), however, results of the RC circuit do not agree with those of S1 because we do not consider parasitic capacitances of G3. As the load capacitances of pMOS and nMOS of G3, Clp and Cln, are 7.73fF and 2.50fF, results of the RC circuit considering the load capacitance agree well with those of the S1 simulation (the last column of Table 2). Therefore, if parasitic capacitances of the driven gate have an enough impact for wire capacitances of the fault location, their effects appear for the voltage at the fault location and the delay time at the primary output.

So far, we have considered open faults at even inversion gates. This means that the initial logic value is the same as one at a primary input. In open faults at odd inversion gates, since equivalent circuits of Figs. 3(a) and 3(b) are exchanged each other (i.e., the circuit of Fig. 3(a) (3(b)) corresponds to VSS (VDD) application.), simulation results of S1 (S2) correspond to VSS (VDD) application for faults at odd inversion gates. Therefore, the proposed method is applicable to open faults at every location of CMOS combinational circuits.

Table 1. Simulation conditions.

Technology	TSMC 0.18μm (MOSIS)
VDD	1.8V
Vtp, Vtn	-0.52V, 0.51V
Gate sizes	L=0.18μm, Wp=3.3μm, Wn=1.0μm
Gate threshold	(1/2)VDD
Rf	100MΩ
Cw1, Cw2	combination of {8fF, 80fF}
t0, t1, t2, t3	0μsec, 5μsec, 25μsec, 45μsec
VDD(t), VSS(t)	(1.8V/20μsec)t, (-1.8V/20μsec)t

Table 2. Simulation results of gate-input open faults.

Sim. No.	Circuit type	Cw1, Cw2 [fF]	Vfmax [mV] (@25ms)	Vfmin [mV] (@45ms)	tpd [μs]	
S1	gate open (f1) VDD application	80, 8	697.9	90.1	6.54	Fig. 6(a)
		8, 8	152.1	0.058	2.05	
		8, 80	127.3	15.9	6.95	Fig. 6(b)
S2	gate open (f1) VSS application	80, 8	-102.3	-11.7	6.93	
		8, 8	-116.3	-0.024	1.99	
		8, 80	-675.6	-83.5	6.54	
S3	Equivalent circuits (Figs. 3(a)&3(b)) *	80, 8	645.8	66.5		
		8, 8	72.0	0.0003		
		8, 80	64.6	6.7		
	Clp=7.73fF ** Cln=2.50fF **	87.73, 10.50	686.5	89.6		
		15.73, 10.50	141.5	0.069		
		15.73, 82.50	123.1	16.1		

*: Vf values are negative for the circuit of Fig. 3(b).
**: Clp and Cln are load capacitances of pMOS and nMOS of G3.

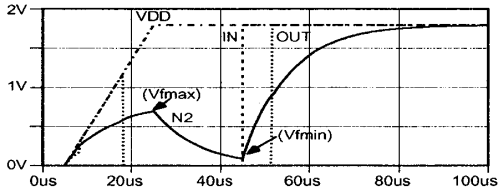

Fig. 6(a). Example of (VDD, Cw1=80fF, Cw2=8fF).

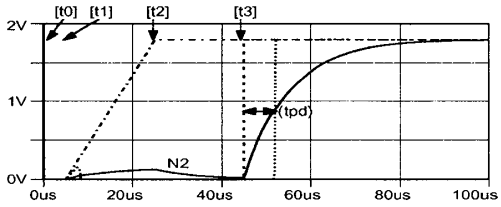

Fig. 6(b). Example of (VDD, Cw1=8fF, Cw2=80fF).

4.1.2 Detection of transistor-input open fault

Now, we consider the transistor-input open faults f2 and f3 as shown in Fig. 1(a). Table 3 shows their simulation results.

Table 3. Simulation results of transistor-input open faults.

Sim. No.	Circuit type	Cw1, Cw2 [fF]	Vfmax [mV] (@25ms)	Vfmin [mV] (@45ms)	tpd [μs]
S4	nMOS open (f2) VDD application	80, 8	654.6	69.5	1.51
		8, 8	79.6	0.0012	0.48
		8, 80	73.4	6.4	1.85
S5	nMOS open (f2) VSS application	80, 8	-88.7	-9.9	0.001
		8, 8	-99.5	-0.34	0.001
		8, 80	-668.6	-73.0	0.001
S6	pMOS open (f3) VDD application	80, 8	693.8	87.8	0.95
		8, 8	143.2	0.40	0.44
		8, 80	124.3	15.4	1.41
S7	pMOS open (f3) VSS application	80, 8	-81.8	-9.1	1.93
		8, 8	-89.0	-0.0053	0.60
		8, 80	-654.4	-76.8	1.58
S8	nMOS open (f2) VDD=+1.0V	80, 8	370.8	39.6	2.89
		8, 8	43.8	0.0006	0.84
		8, 80	43.4	4.6	3.21
S9	nMOS open (f2) VDD=+1.8V VSB=+1.0V	80, 8	679.1	89.7	3.01
		8, 8	78.7	0.0011	0.79
		8, 80	80.4	8.4	3.34

Comparing simulation results of S4 to S7, the positive power supply application S4 is suitable for detecting the nMOS open fault, and the negative voltage application S7 is suitable for the pMOS open detection. This phenomenon is explained as follows. Assuming the nMOS open fault, the pMOS transistor functions normally. In the positive power supply application, since the initial value is logic 0, then pMOS/nMOS=on/off. During the testing interval, logic value 1 is assigned to the gate with the fault. At this time, the pMOS transistor becomes the off-state normally; however, the nMOS transistor is difficult to be the on-state because of the fault. Then, the time of the gate output to transit from 1 to 0 becomes long. For the pMOS open fault, we can explain by the same way as the above.

Values of delay times of transistor-input open faults are smaller than those of gate-input open fault because the complement transistor fed by the same interconnect functions normally. In order to increase the delay time, it is possible to apply two methods: very-low-voltage testing [15] and application of the substrate bias VSB [10], [13]. In the simulation S8, the positive power supply voltage is reduced to 1.0V, which corresponds to twice the transistor threshold voltage (2Vt). The delay times increase by 74% to 91% comparing with those of the nominal power supply voltage of simulation S4. Moreover, if we apply the substrate bias VSB of 1.0V under the nominal power supply (simulation S9), we can obtain the similar effect. The delay times increase by 81% to 99%. From the above two methods, reducing the power supply voltage gives the same effect as increasing the substrate bias voltage. Application of these two methods is easy because they can apply by controlling only power supply voltages as well as VDD and VSS controlling.

4.2 Plan of testing

(1) To prevent rapid voltage change at the fault location, it is better to apply the ramp voltage with a more gentle slope or to delay the application timing of a test vector. This means that we can determine the slope of the ramp voltage if maximum values of a fault resistance and wire capacitances which we intend to detect are set up in advance. Besides, if we observe a circuit output at appropriate time, the proposed method can apply to an open fault with a small time constant (i.e., a fault with a small resistance and wire capacitance).

(2) Since the voltage stability of the fault location depends on both the balance between Cw1 and Cw2 and the positive/negative of the applying power supply voltage, we have to examine two methods of the voltage application for each location (i.e., Figs. 5(a) and 5(b)). These two methods give good results for both the gate-input open fault and the transistor-input open fault.

(3) In the proposed method, the initial logic value at the fault location is automatically assigned when the ramp voltage is applied. Then, only one test vector is needed, which has to propagate a logic value to the primary output for detecting the open fault as a signal delay or an error value. Therefore, test generation algorithm and complexity are just the same as those for stuck-at faults. Moreover, open faults on the same sensitizing path are tested simultaneously.

5. Conclusions

We proposed a simple method for detecting open faults by logic testing. If we firstly set all terminals of the circuit to the GND level, all nodes in the circuit are also set to the fixed GND level. Next, after we carefully apply the ramp voltage to the power supply terminal, we can detect the open fault as a signal delay by assigning an appropriate logic value to the fault location. We showed the effectiveness of the method by using circuit simulation. In order to show practicality, we further need to estimate a testing cost and try to apply to sequential circuits.

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