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A Unified Procedure to Overcome the Byzantine General's Problem for Inter-gate and Intra-gate Bridging Faults in CMOS Circuits

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In this paper, we present two algorithms, which can be used to overcome the Byzantine General's problem for bridging faults during the fault simulation and test pattern generation. The first algorithm applies to hard short bridging faults, and the other applies to resistive bridging faults. These algorithms apply to inter-gate and intra-gate bridging fault. By using these propose algorithms, the usual comparison between the intermediate potential and the logic threshold of the driven gates is replaced by the comparison between the equivalent resistance of the pull-up and pull-down conducting transistors. Moreover, the algorithm is much faster since no spice simulation is required. The accuracy is of ± 0.01 V to compare with SPICE simulation for hard short bridging fault and ± 0.2 V for resistive bridging fault in the interval of intermediate voltage.

1. Introduction

It is known that the bridging faults (BFs) are the major failure source of the VLSI circuits. This kind of fault is due to the failure of two or more leads unintentionally shorted. This defect causes different behavior to the faulty circuits depending on the value of the bridging resistance[1]. Traditionally, bridges have been regarded as shorts connecting two or more nodes through a path with a resistance equal to zero.

More recently, the possibility of a higher resistance for a bridging defect has been taken into account. It has been shown that a bridging fault is hard to be modeled using the stuck-at fault model[2]. There are two testing methodologies being used to test bridging faults. First, a logic/function test technique that determine test results by measuring the output voltage of CUT or validate the correct operation of a system with respect to its functional specification for most complex circuits such as microprocessor[3]. The faulty behavior of a gate with a bridging fault can be determined using simulation and the results can be used to sensitize the gate's inputs to the output. Second, I_{DDQ} testing technique determines the test results by monitoring quiescent supply current of CUT[4]. It is a basic assumption to generate the I_{DDQ} testing sets that two nodes with opposite logic are connected together.

The resistance of a bridge fault is critical in determining whether the fault can be detected; if the resistance is too high, the fault will not cause an error at the output during functional testing or abnormal I_{DDQ} during I_{DDQ} testing. In addition, if the bridge resistance is assumed very low, incorrect diagnoses might occur if the logic threshold values for gates driven by one output of the two-bridged gates are not the same, and if the logic levels for these gates are therefore interpreted differently. This scenario is referred to as the Byzantine General's problem[5].

A few works have been done to face the Byzantine General's problem such as the works in Refs. 6) and 7). Renovell, et al.[6] proposed complex calculation model to collapse P and N network transistors based on the concept of mean value to evaluate the bridging voltages. Moreover this work did not address the resistive bridging faults. Lee, et al.[7] proposed another solution for Byzantine General's problem for a resistive bridging fault by using an iteration method, and assumed a calibrating factor to collapse P and N network transistors which achieved accuracy outside the interval of intermediate. The accuracy of this procedure depends on more iterations. Indeed, more accuracy of evaluating a bridging voltage in the interval of occurence intermediate voltage is necessarily. In this paper, we will provide a more accurate result from previous works, especially in the interval of occurrence intermediate voltage (2–3) V. Moreover for the resistive BF we determine the interval of intermediate voltage by the relation between the resistance of BF and the equivalent resistance of the pull-up

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(Rpeq.) or pull-down (Rneq.) networks. Our method achieves more accuracy by using simple calculation that uses the determination of the relation between the resistances of pull-up and pull-down networks for hard short and resistive BFs. Moreover, the method doesn't need the use of iterative method and SPICE simulation to overcome Byzantine General's problem in hard short and resistive BFs.

A preliminary version of this work has been proposed in Ref. 8). This paper is organized as follows. Section 2 describes the bridging fault model and the Byzantine General's problems for inter-gate and intra-gate BF. Sections 3 and 4 describe hard-short and resistive bridging fault simulation, and present two algorithms to overcome the Byzantine General's problem. Finally, Section 5 presents the conclusions.

2. Preliminary

2.1 Bridging Fault Model

Bridging faults occur when two or more electrically distinct nodes of the circuit get connected due to a defect. Some bridges occur when dust or extra material is deposited during fabrication. The result is that two distinct nodes on the same gate get connected. Circuit nodes on two adjacent gates can also get shorted as shown in **Fig. 1** (a), while Fig. 1 (b) shows that the transistor level of the bridging gates. Most of the early approaches have used the classical stuck-at-0/1 fault model for intra-gate bridging and wired logic for inter-gate bridging.

To detect a bridging fault between X and Y nodes, that nodes must be set to opposite values, for example X set to 1 (0) and Y set to 0 (1) and the voltage of the faulty nodes must be sensitized to an output. According to the effect of resistance Rf and the effect of the driving gate the bridging lines can have intermediate voltage values V_X and V_Y (not well defined logic values of 1 or 0). In order to simulate the effects of a bridging fault it is necessary to determine the intermediate voltage of the shorted nodes and compare it to the logic threshold voltage of the driven gates. Possibly leading to logic errors when the downstream of logic gates from the bridge nodes can have different input logic thresholds. Thus the intermediate voltage at a bridged node may be interpreted differently by different gates. This is known as the Byzantine General's problem. In steady state conditions, the detectability of this kind of fault can be determined only by correctly evaluating the position of the intermediate voltage with respect to the logic threshold of the driven gate[7].

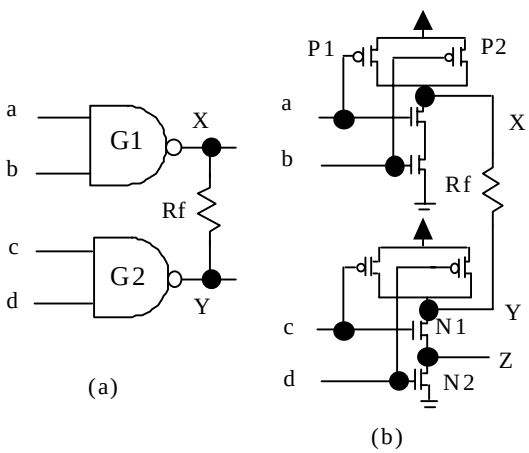

Fig. 1 External bridging fault.

We next define some terminology. A node which is either an input or an output of a gate is an external node of the gate. In Fig. 1, a, b and X are the external nodes of gate G1. Other nodes of the gate, such as Z of gate G2 in Fig. 1 (b) are internal nodes. Shorts between nodes of two different CMOS gates are inter-gate BF's. Inter-gate BF's can occur between the external nodes of two gates (X and Y bridge in Fig. 1 (a)) and are known as external BF's. Inter-gate BF's can also involve one internal node of a gate. Note that this does not take some faults into account, such as BF between internal nodes of different gates, because usually the probability of their occurrence is negligible[9]. BFs involving only nodes of one gate are intra-gate BF's (X and Y bridge in Fig. 3). If the bridge resistance is small then it is a hard short BF else it is a resistive BF. Our target in this work is to propose a unified procedure to solve Byzantine General's problem for inter-gate and intra-gate BF's.

2.2 Byzantine General's Problem (BGp)

Byzantine fault behavior means that an intermediate value within a certain interval may be interpreted as different logic values by different gates owing to the variation in threshold voltage between different gate types. An inter-gate bridging fault is illustrated in **Fig. 2** where the outputs of both a NAND and a NOR gates are shorted together. An intra-gate bridging fault is illustrated in **Fig. 3** where nodes X and Y of an AOI (AND-OR-INVERTER) are shorted to-

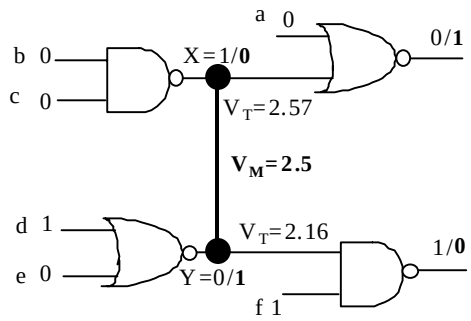

Fig. 2 Example of BGp for inter-gate BF.

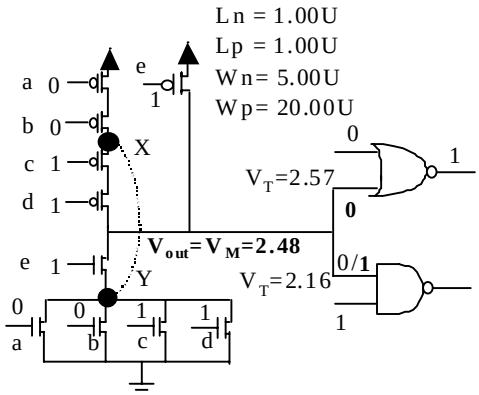

Fig. 3 Example of BGp for intra-gate BF.

gether. The logic thresholds of the driven gates are indicated in the figures.

In Fig. 2, when the input vector is $(a, b, c, d, e, f) = (0, 0, 0, 1, 0, 1)$, in the fault free circuit the output of the X and Y nodes would be '1' and '0' respectively. Assuming a low resistance (10 ohm) short, V_X=V_Y=V_M, and the SPICE simulation shows that the intermediate output voltage (V_M) is 2.5 V. This intermediate voltage must be now compared to the logic threshold voltage (V_T) of the driven gates.

Assume that the input of the NOR gate has a logic threshold voltage V_T equals 2.57 V and the threshold input of the NAND gate equals 2.16 V. In this condition, the faulty input of NOR gate interprets the voltage V_M as a logic '0' ($X = 0$), and the faulty input of NAND gate interprets V_M as a logic '1' ($Y = 1$) as shown in Fig. 2 Taking into account the logic threshold of the driven gate, it is clear that the bridging cannot be modeled using wired logic. In Fig. 3, the same phenomenon can be observed for intra-gate AOI ($Vout = \overline{(a + b + c + d)e}$). Taking into account the logic threshold of the driven gate, it clearly appears that the bridging

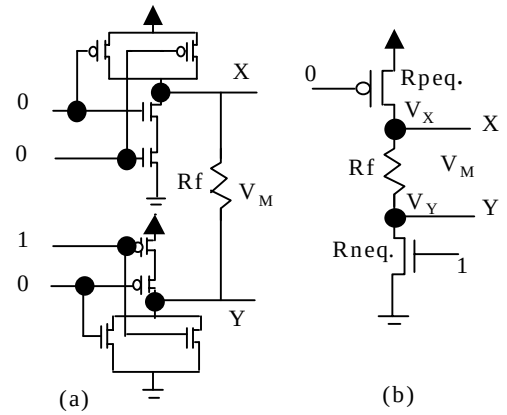

Fig. 4 BF for CMOS gate.

cannot be viewed as a stuck-at fault.

These two small examples clearly illustrate the problem of realistic fault model for inter-gate and intra-gate BF's. In the next sections, we simulate the BF in the case of Rf is very low and other cases when Rf has different values compared with the channel resistance of the conducting transistors.

3. Hard Short BF Simulation

The general problem of the BF can now be expressed as follows:

(1) Determine V_M between the P and N conducting transistor networks,

(2) Compare V_M with the known V_T of the driven gate.

Figure 4 shows the general structure of BF in Fig. 2 when applied $(0, 0, 1, 0)$ on (b, c, d, e). The transistor level BF is shown in Fig. 4 (a), and the equivalent conducting transistors have been represented in Fig. 4 (b), where Rpeq. and Rneq. are the equivalent resistance of the conducting transistor in pull-up (Pnet.) and pull-down (Nnet.) networks.

There are four cases for (Pnet., Nnet.): (saturation, saturation), (linear, saturation), (saturation, linear), (linear, linear). For Pnet. to saturate, we must have $Vgd > V_{Tp}$, then $V_{IN} - V_X > V_{Tp}$. Substituting the values of V_{IN} (0 V), and V_{Tp} (−0.75 V) into this equation, we obtain $V_X < 0.75$ V. If Pnet. is in the linear region then $V_X > 0.75$ V and may have intermediate voltage. Similarly if Nnet. is in the linear (saturation) region then $V_Y < (>)\, 4.25$ V at V_{Tn} (0.75 V). The voltage ranges with respect to the four cases are shown in **Table 1** and the estimation of intermediate voltage on V_X and V_Y. The Lin. (Sat.) is abbreviation of

Table 1 Estimation of occurence of BGp.

Pnet.	Nnet.	V_X	V_Y	BGp for hard short BF
Sat.	Sat.	<0.75V	>4.25V	0
Lin.	Sat.	>0.75V	>4.25V	0
Sat.	Lin.	<0.75V	<4.25V	0
Lin.	Lin.	>0.75V	<4.25V	(V_X & V_Y) V_X or V_Y or both*

* Estimation of BGp for a resistive BF

linear (saturation) region. The estimation V_X (V_Y) means that the Byzantine General's problem may occur on the faulty node X (Y), and 0 means that the Byzantine General's problem does not occur.

We assumed that the resistance of channel for pull-up transistor (Pnet.) equals the resistance of channel for pull-down transistor (Nnet.). When '$Rf = 0$' or is very low (10 ohm), it is possible to write the equality of the source-to-drain current for the P (Isdp) and the drain-to-source current for the N (Idsn) transistors as shown in Fig. 4, and both V_X and V_Y are equal to V_M. The following equation is obtained

$$\frac{\text{VDD} - V_M}{\text{Rpeq.}} = \frac{V_M}{\text{Rneq.}}, \text{then}$$
$$\frac{V_M}{\text{VDD} - V_M} = \frac{\text{Rneq.}}{\text{Rpeq.}}. \quad (1)$$

From the CMOS process parameters, we approximate the drain-to-source resistance for linear Nmos and Pmos transistors by Ref. 10),

$$Rn = \frac{1}{\beta_n(\text{VDD} - V_{T_n})}, Rp = \frac{1}{\beta_p(\text{VDD} - |V_{T_p}|)}.$$

Note that both Rn and Rp are inversely proportional to (W/L); increasing the aspect ratio decreases the equivalent resistance. The resolution of these equations could give the value of V_M as a function of the CMOS parameters βp, βn, V_{Tp}, and V_{Tn}. Where β and V_{Tp} (V_{Tp}) is device transconductance value and P(N) transistor threshold, $\beta = K(W/L)$ where K is process transconductance.

Equivalent resistance of parallel and serial transistors can be calculated by using the following equation,

$$R_{eq.} = \frac{1}{\beta_{eq.}(\text{VDD} - V_{T_M})}.$$

Where V_{T_M} is the mean value of the threshold of serial or paralell networks, $\beta_{eq.}$ for paralell nertwork will be

$$\beta_{eq.} = \sum_{i=1}^{n} \beta_i.$$

and $\beta_{eq.}$ for serial network can be approximated as

$$\frac{1}{\beta_{eq.}} = \sum_{i=1}^{n} \frac{1}{\beta_i}.$$

However for a serial network this deviation is done based on the assumption of neglect the body effect and the transistor connected to VDD or GND is at the saturation region[7]. This conflicts with the fact that transistors involving in bridging faults are likely to operate in a linear region. The experimental data in Ref. 7) shows that a calibrating factor 0.75 for both P and N serial networks should be multiplied to the above equation to achive high accuracy. Then the above equation will be

$$\frac{1}{\beta_{eq.}} = 0.75 \sum_{i=1}^{n} \frac{1}{\beta_i}.$$

By taking into account this calibrating factor on Eq. (1), then Eq. (1) will be

$$\frac{V_M}{\text{VDD} - V_M} = \frac{\text{Rneq.}}{0.75\text{Rpeq.}}. \quad (2)$$

According to the simulation results in the previous work in determination of the threshold for CMOS gates[11], we consider the interval [2, 3] V for VDD = 5 V for the intermediate value. Faults resulting in voltages outside that interval are considered to be interpreted as normal logical values regardless of parameter variations and Byzantine fault behavior. Table 1 shows the intermediate voltage is occured when the transistors are linear, and also our work in Ref. 8) shows that the occurence of intermediate voltage in hard short BF occurs only when Rpeq. = Rneq. or even very close as shown in **Fig. 5**. The simulation results for different circuits show that by using Eq. (1) in the interval of intermediate voltage is more accuracy from using Eq. (2). Outside the interval of intermediate voltage the Eq. (2) is more accuracy (see Fig. 7). When Rneq. = Rpeq. as shown in Fig. 2 we have

$$\frac{V_M}{\text{VDD} - V_M} = \frac{\text{Rneq.}}{\text{Rpeq.}} = 1.$$

We define Rneq./Rpeq. by R_{Int}, and $R_{Th} = V_T/(\text{VDD} - V_T)$ as the value of R_{Int} which produce $V_M = V_T$. As previously mentioned the

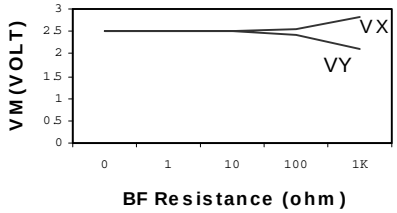

Fig. 5 External BF between NAND and NOR.

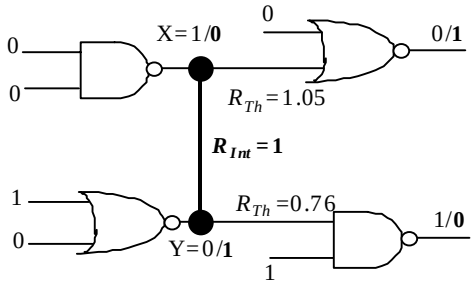

Fig. 6 R_{Int} and R_{Th} operation for inter-gate BF.

logic behavior of the BF is deduced from the comparison between the intermediate bridge voltage V_M and the logic threshold voltage V_T of the driven gates. The basic and very simple principle is: For a driven gate,

if $V_M(R_{Int}) > V_T$ (R_{Th}) then $X = Y = 1$,

if $V_M(R_{Int}) < V_T$ (R_{Th}) then $X = Y = 0$.

Figure 2 shows the value of V_T of the input NOR = 2.57 and R_{Th} which equals $V_T/(\text{VDD}-V_T) > 1$; according to the last principle we find $V_M < V_T$ then $X = 0$. In the case of V_T of the input of NAND gate = 2.16 and $V_T/(\text{VDD} - V_T) < 1$ then $V_M > V_T$; $Y = 1$ as illustrated in **Fig. 6**.

It is now possible to describe the global procedure to detect the bridging faults using Eq. (1) for the relation between R_{Int} and R_{Th}. Note that the procedure is very simple and does not need SPICE simulation. It can be represented by the following algorithm:

For each external/internal inter-gate or intra-gate bridging between X, Y nodes
Do begin
-From the logic values present on the gates, determine the transistor connectivity
-Replace all series conducting transistors with an equivalent one
-Replace all parallel conducting transistors with an equivalent one
-Compute R_{Int}=Rneq./Rpeq.
- **For each driven gate input do begin**
- Compute R_{Th} from V_T of a driven gate
- If $R_{Int} > R_{Th}$ then node=1; else node=0
- **End**

End

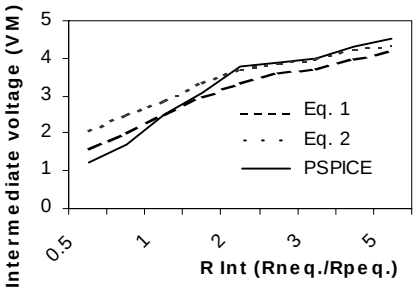

Fig. 7 Validation of our algorithm.

In order to validate the previous algorithm, the external bridging between 3-NAND and 4-NAND have been simulated and compared as shown in **Fig. 7**, which gives the intermediate voltage V_M versus R_{Int} (Rneq./Rpeq.) characteristics for external BF by using Eq. (1) and Eq. (2). We observe that the agreement is extremely good between the PSPICE simulation result and our algorithm whatever the resulting voltage V_M especially in the interval of intermediate voltage (2–3) V, which leads to Byzantine General's problem. The accuracy in this interval is more important than other interval. For example, (0–2) V is considered as logic 0 and (3–5) V is considered as logic 1. In Fig. 7 the worst case of Eq. (1) presents a difference of ± 0.01 V (± 0.08 V) inside (outside) the interval of intermediate between the simulation results and our algorithm which represents an excellent accuracy in the interval of intermediate. The worst case of Eq. (2) presents a difference of ± 0.16 V (± 0.01 V) inside (outside) the interval of intermediate, which is a very acceptable accuracy outside the interval of intermediate.

4. Resistive BF Simulation

In this section, we first assume the P-network and the N-network are only composed of a single transistor. **Figure 8** illustrates the faulty situation with a single N and P conducting transistors according to the different cases of Table 1. The demonstration will be extended to serial and parallel transistors by using an equivalent resistance instead of a single resistance. Hence for the resistive BF (Fig. 8) we have $I_{sdp} \cong I_{dsn} \cong I_{Rf}$, and then

$$\frac{\text{VDD} - V_X}{Rp} = \frac{V_Y}{Rn} = \frac{V_X - V_Y}{Rf}. \qquad (3)$$

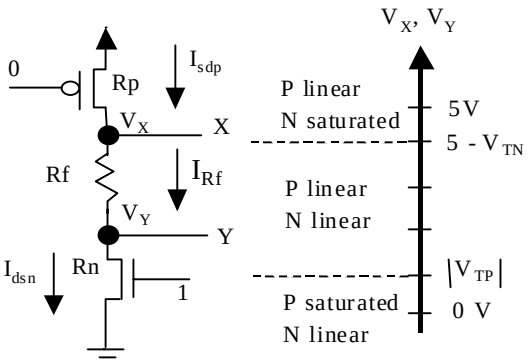

Fig. 8 Single transistor case.

According to Table 1 and Eq. (3), we next discuss the four possible cases for P and N transistors.

1: (P, N) = (saturation, saturation)

From Table 1, we have $V_X < 0.75\,\mathrm{V}$ and $V_Y > 4.25\,\mathrm{V}$. Since it contradicts to $V_X > V_Y$, this condition is impossible.

2: (P, N) = (linear, saturation)

From Table 1 and Fig. 8, we have $V_X > 0.75\,\mathrm{V}$ and $V_Y > 4.25\,\mathrm{V}$. Since $V_X > V_Y$, we have $V_X > 4.25\,\mathrm{V}$. From Eq. (3), we have

$$V_X - V_Y = \frac{Rf(\mathrm{VDD} - V_X)}{Rp} \qquad (4)$$

and

$$V_X - V_Y = \frac{Rf(V_Y)}{Rn}. \qquad (5)$$

Dividing Eq. (4) by Eq. (5), we obtain

$$V_X = \mathrm{VDD} - V_Y(Rp/Rn) > 4.25.$$

Substituting V_Y when N transistor is saturated by 4.25 we have

$$Rn/Rp > 5.6$$

Clearly the ratio more than 5.6 may not be used for most logic circuits, hence this condition is very weak. If this condition occurs, then since both V_X and V_Y are greater than 4.25 V, they both have a logic 1, and intermediate voltage does not occur. Therefore this condition results in a wired-OR logic. Note that Rf is cancelled out when dividing Eq. (4) by Eq. (5). Therefore the ratio $Rn/Rp > 5.6$ provides a quick method to determine whether this case can occur or not, and this greatly simplifies the test generation or fault simulation process.

3: (P, N) = (saturation, linear)

From Table 1 and Fig. 8, both V_X and V_Y are smaller than 0.75 V in this case. Using a similar derivation as in the previous case, we obtain

$$V_Y = (Rp/Rn)(\mathrm{VDD} - V_X) < 0.75.$$

For $V_X = 0.75\,\mathrm{V}$ at saturated we have

$$Rn/Rp < 0.18.$$

Although this condition is also very weak since in general the value of Rn/Rp is taken between 2 and 3 in logic circuits for reason of balanced rising/falling times, this case may not occur as the previous case. Hence this case results in a wired-AND logic, and intermediate voltage does not occur. In our system we can also check out the condition quickly without considering the value Rf.

4: (P, N) = (Linear, linear)

According to Table 1 and Fig. 8, $V_X > 0.75\,\mathrm{V}$ and $V_Y < 4.25\,\mathrm{V}$. In this case we can say the ratio Rn/Rp is

$$0.18 < Rn/Rp < 5.6.$$

The estimation of occurrence of intermediate voltage in this condition is more likely than the previous conditions. Therefore, next we discuss in detail with the general case of Eq. (3). according to the design of CMOS circuits. We assumed three cases for the value of channel resistance of pull up and pull down networks, which are (i) Rpeq. = Rneq., (ii) Rpeq. > Rneq. and (iii) Rpeq. < Rneq. Hence for the resistive BF the general case of Eq. (3) becomes

$$\frac{\mathrm{VDD} - V_X}{\mathrm{Rpeq.}} = \frac{V_Y}{\mathrm{Rneq.}} = \frac{V_X - V_Y}{Rf}. \qquad (6)$$

We can obtain on three initial conditions for V_X and V_Y according to the relation between Rpeq. and Rneq.;

(i) Rpeq. = Rneq., then$\mathrm{VDD} - V_X = V_Y$,
(ii) Rpeq. = 2Rneq., then$\mathrm{VDD} - V_X = 2\,V_Y$,
(iii) Rneq. = 2Rpeq., then$\mathrm{VDD} - V_X = V_Y/2$.

The initial condition of Case (i) means that both V_X and V_Y have intermediate voltage at low resistive BF. The value of V_Y is inversely proportional to Rf (increasing of the Rf decreases V_Y), and vice versa for V_X. From Eq. (6), we can find the relation between Rf and Rpeq. (Rneq.) as follows:

$$\frac{V_X - V_Y}{\mathrm{VDD} - V_X} = \frac{Rf}{\mathrm{Rpeq.}}. \qquad (7)$$

As we have mentioned above we choose $V_X = 3\,\mathrm{V}$ and $V_Y = 2\,\mathrm{V}$ for the interval of intermediate voltage. Substituting these values of V_X and V_Y in Eq. (7), we can obtain on the critical value of Rf, which equals 0.5 Rpeq. (Rneq.). For more than 0.5 Rpeq., $V_X(V_Y)$ is equal to logic 1 (0).

Case (ii) is inverse of (iii), but Case (iii) is more realistic than (ii). Thus in the case of Rpeq. < Rneq. (Rneq. = 2 Rpeq.), the initial

condition as mentioned above is VDD $- V_X = V_Y/2$. The interpretation of this initial condition is that both values of V_X and V_Y have the high value ($\cong 3.33$ V) at the starting point. When the value of Rf increases V_Y will decrease and may be the intermediate value, and V_X will increase more. Therefore, when Rf increases and Rneq. equals two times of Rpeq., then from Eq. (6) we obtain

$$\frac{V_X - V_Y}{V_Y} = \frac{Rf}{2\,\text{Rpeq.}}. \tag{8}$$

Substituting V_X from the initial condition (iii) and V_Y by 3 V in Eq. (8), we obtain on the critical value of Rf that equals one third (1/3) of Rpeq. Similarly, when V_Y is equal to 2 V, we obtain Rf that is equal to 2 Rpeq. Thus the value of V_X has logic 1 for all values of Rf and V_Y has intermediate value in the interval of Rf that is equal to [1/3–2] Rpeq. and larger (lower) than this value for $V_Y = 0(1)$.

In general case for Rneq. $= m$Rpeq., where $m > 1$, the V_Y has intermediate value in the interval of Rf that is equal to $[(2m/3 - 1) \sim (3m/2 - 1)]$Rpeq. Note that Case (ii) is the opposite of (iii). Thus in (ii) the value of V_Y has logic 0 for all values of Rf and V_X has intermediate value in the interval of Rf equals [1/3–2]Rneq., (in general $[(2m/3 - 1) \sim (3m/2 - 1)]$ Rneq.), and larger (lower) than this value $V_X = 1(0)$.

However, the PSPICE simulations have been done on Eq. (6) for a variety of BFs to verify the accuracy of our algorithm. The plotting of voltage on X and Y nodes as a function of Rf relative to Rpeq. for Rpeq. $=$ Rneq. and Rneq. $=$ 2 Rpeq. as shown in **Fig. 9**. and **Fig. 10** respectively. Figure 9 shows the external BF between 2-NAND and 2-NOR gates when Rp equals Rn and the internal BF between two 2-NAND gates when Rp equals $2Rn$, but in both cases Rpeq. equals Rneq., and we find that when Rf is very low, V_X and V_Y have intermediate voltage until Rf equals 0.5 Rpeq. Above that value we have shown that V_X equals logic 1 and V_Y equals logic 0.

Figure 10 shows the external bridge between two 2-NAND gates when Rpeq. $<$ Rneq. and $m = 2$. The value of V_X has logic 1 for all values of Rf and V_Y has intermediate value in the interval of Rf is equal to [1/3–2]Rpeq., and larger (lower) than this value $V_Y = 0(1)$. From Figs. 9 and 10 the maximum deviations from the PSPICE simulations is ± 0.2 V when Rpeq.

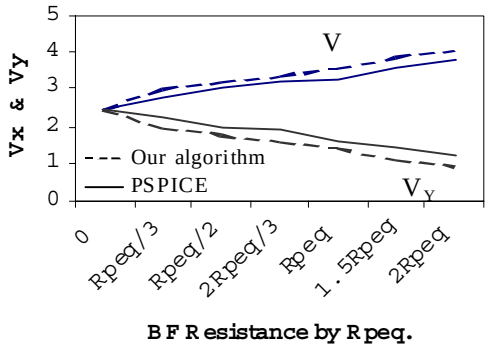

Fig. 9 Simulation of resistive BF for Rpeq. = Rneq.

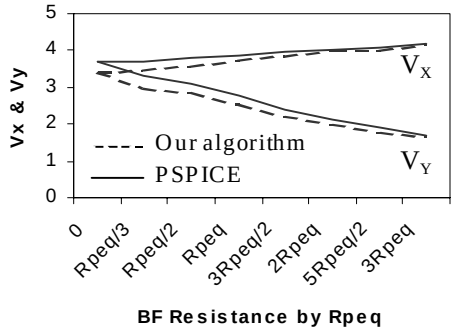

Fig. 10 Simulation of resistive BF for Rneq = 2 Rpeq.

$=$ Rneq. and -0.2 V when Rneq. $= 2$ Rpeq.

It is possible now to describe the second algorithm to test bridging faults for different values of Rf as follow:

For each external/internal inter-gate or intra-gate bridging between X, Y nodes Do begin

-From the logic values present on the gates, determine the transistor connectivity

-Replace all series conducting transistors with an equivalent one

-Replace all parallel conducting transistors with an equivalent one

- **For pull up/down network do begin**

-Compare Rpeq. and Rneq.

-If Rpeq. $=$ Rneq., $Rf \geq$Rpeq./2, then $V_X = H$, $V_Y = L$,

-If Rneq. $= m$Rpeq., and $Rf < [2m/3 - 1]$Rpeq., then $V_X = V_Y = H$,

-If Rneq. $= m$Rpeq., and $Rf \geq [3m/2 - 1]$Rpeq., then $V_Y = L$, $V_X = H$,

-If Rpeq. $= m$Rneq., and $Rf < [2m/3 - 1]$Rneq., then $V_X = V_Y = L$,

-If Rpeq. $= m$Rneq., and $Rf \geq [3m/2 - 1]$Rneq., then $V_X = H$, $V_Y = L$,

- **For each driven gate i/p do begin**

-Compute V_X and V_Y) by Eq. (6)
-If either V_X or $V_Y > V_T$ then node = 1; else node = 0
- **End**
- **End**
End

Finally, we can summarize that the resistive bridging voltage calculation by checking the ratio Rneq./Rpeq., the function of BF is evaluated in one of the following cases:
1. (Rneq./Rpeq.) > 5.6: a wired-OR logic is adopted.
2. (Rneq./Rpeq.) < 0.18: a wired-AND logic is used.
3. 0.18 < (Rneq./Rpeq.) < 5.6: the last algorithm is used.

5. Conclusions

In this paper we have presented two algorithms which can be used to determine if a particular structure of transistors gives an intermediate voltage which is higher or lower than a given threshold voltage of a driven gate. These algorithms applied to hard short and resistive BF for both inter-gate and intra-gate BF. We have performed the simulation to verify our work. The worst case presented a difference of ±0.01 V for hard short BF and ±0.2 V for resistive BF in the interval of intermediate [2, 3] V between the simulation results and our algorithms. It should be recalled that these proposed algorithms allow to overcome the Byzantine General's problem for the bridging faults with the accuracy of SPICE simulations and a negligible effort since neither pre-simulation (such as preparing the circuits under simulation by entering parameters for each component) nor iterative procedure are required, compared to previously published methods.

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