Transistor Computer ETL Mark V

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1. *Introduction*

The ETL Mark V is a general-purpose decimal digital computer, operating throughout in the serial mode at a digit frequency of 230 kc/s, and using a magnetic drum as its storage. It is based on the ETL Mark IV computer, which was developed by a research group of the Electrotechnical Laboratory and has had a successful career since it was built in 1957.

The ETL Mark V utilizing approximately 1,700 transistors and 20,000 diodes was constructed by the Hitachi, Ltd.

Details are given of the system and logical design of the ETL Mark V in this paper.

2. *Word Formats*

The computer is a decimal serio-parallel computer. The word length is 12 decimal digits, each being represented in the conventional 8–4–2–1 code. 11 digits are used for a fixed point number and 1 digit for its sign. For a floating point number, 9 digits are used for the mantissa, 2 digits for the exponent and 1 digit for their signs as shown in Fig. 1. Negative numbers are represented by their complements with respect to ten.

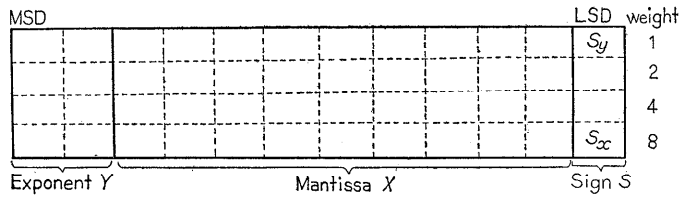

Fig. 1. Format of the floating point number word

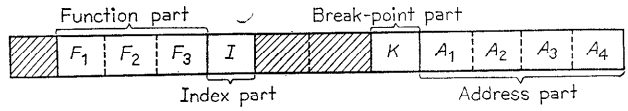

Fig. 2. Format of the instruction word

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An instruction, as shown in Fig. 2, is made up of 3 F-digits indicating the function of the instruction, 1 I-digit referring to the index registers, 1 K-digit indicating a break-point stop, 4 A-digits allowing 10,000 addresses in the memory (only 4,200 addresses being used), and the other 3 gap digits. The address can be modified by a single or two index registers designated in the I-digit.

In order to represent the alphabet, 2 digits are assigned to each character. Thus up to 5 characters can be contained in a word.

3. *Arithmetic Unit*

The arithmetic unit for the ETL Mark V incorporates both fixed point and floating point arithmetic facilities intending for scientific computation. It consists of an adder, a normalizing unit and five registers which are an upper and a lower accumulator, a multiplier-quotient register, a multiplicand-divisor register and a buffer register. The arithmetic operations are always performed in double length, so that double-precision arithmetic operations are easily carried out even on the floating point numbers. Table 1 shows a few examples of the program steps for the double-precision floating point arithmetic operations including transfer of information to the memory. The speeds for the typical arithmetic operations are shown in Table 2. These speeds exclude the time to extract the instructions or to fetch the operands.

Table 1. Examples of the program steps

	Single	Double
Addition	3	6
Multiplication	3	7
Division	3	15

Table 2. Speeds for the typical arithmetic operations

Operations	Speeds (ms)	
	fixed point	floating point
Addition and Subtraction	0.47	0.62
Multiplication (average)	6.6	5.7
Division (average)	7.8	5.9
Jump	0.16	0.16

4. *Control*

The computer is synchronized with the clock pulses of 230 kc/s read from a timing track on the magnetic drum, and is controlled serially. However, a particular technique to shift the content of the accumulators is adopted for speeding up the arithmetic operations. It permits one digit shift in one clock pulse duration.

The output operations are performed concurrently with the other internal operations. On receipt of an output instruction the control takes out the content of the buffer register to the selected output device. If another transfer instruction to the buffer register or output instruction is encountered before the completion of the previous output operations, the computer is held up until the output is free to accept the new information.

All the memory operations and input-output characters are parity-checked respectively.

5. *Memory*

A medium-speed magnetic drum is employed for the storage. The drum has 4,200-word capacity and is divided into twenty 200-word and four 50-word bands, each consisting of 5 tracks corresponding to the 8–4–2–1 information bits and a parity bit. The 200-word bands are used in a normal way with 5.2 ms average access time. The 50-word bands are provided for the quick-access storage. The average access time is 1.3 ms that is four times as fast as that of the normal bands.

In writing information the Return-to-Zero method is adopted with 3.1 bits/mm packing density.

6. *Input-Output*

The information channel to the computer is via either one of two 200-character/sec photo-electric paper-tape readers or a flexo-writer operating at 10-character/sec. The information to be inserted is punched on 8-unit paper-tape and read directly into the least significant digit of the upper accumulator, and then automatic shift-up facility allows successive read-in operations in excecuting an input instruction.

The output information is taken from the upper accumulator through the buffer register to either one of two 30-character/sec paper-tape punches or to the flexo-writer.