社団法人 情報処理学会 研究報告
IPSJ SIG Technical Reports

2008－SLDM－135（9）
2008／5／9

Analysis of Effects of Input Arrival Time Variations on On-Chip Bus Power Consumption

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あらまし 本稿では，入力信号の到着時間がばらついているときのオンチップバスの電力を解析する．プロセスの寸法が縮小するに従い，配線間のカップリング容量の充放電による電力消費（カップリング電力）が大きくなっている．カップリング電力は隣り合う配線の信号遷移のタイプおよび信号の相対的な遷移時間差に依存して決まる．既存の電力見積もりでは，入力信号の到着時間は決定論的に扱われてきた．我々はプロセスばらつきなどの影響を考慮した非決定論的な入力信号の到着時間を扱う．解析とシミュレーションの結果から以下の事実を得た．(1) 入力信号の到着時間のばらつきがあり，かつ同相遷移の逆相遷移に対する出現確率が大きく異なる場合には，カップリング電力の値がこれまでの見積もりとは大きく異なる．(2) 同相や逆相の遷移を抑える低電力バス符号化を使うことは，電力の削減だけでなく信号到着時間のばらつきがカップリング電力に与える影響の緩和にも役立つ．

キーワード 入力信号到着時間のばらつき，オンチップバス，カップリング電力，電力見積もり，低電力バス符号化

Analysis of Effects of Input Arrival Time Variations on On-Chip Bus Power Consumption

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Abstract This paper describes analysis of on-chip bus power in the presence of arrival time variations of input signals. With shrinking process geometries, coupling power between neighboring bus lines has enlarged. The coupling power depends on not only signal transition type but also the relative signal transition time difference. For conventional dynamic power estimation, deterministic models of the time difference are assumed. We deal with nondeterministic models such as process variations, because these variations cause the input arrival time variations. As a result, the arrival time variations increase power estimation error. In our analysis and experiments, following results are presented. 1) When there are both the arrival time variations and unbalanced occurrence probability of similarly switching compared with oppositely switching, the power estimation error is large. 2) Bus coding, which reduces similarly and/or oppositely switching, has beneficial effects on both power reduction and the error reduction.

Key words input arrival time variation, on-chip bus, coupling power, power estiamtion, low power bus coding

1. Introduction

Power dissipation is a limiting factor for current and also future technologies. With the progress of deep sub-micron technologies, shrinking geometries have led to a reduction in the self capacitance of wires. However, coupling capacitances have increased as wires have a larger aspect ratio and are brought closer together. The lateral component of interconnect capacitance (coupling capacitance) will continually grow to dominate the total interconnect capacitance due to the reduction in wire pitch and the increase in the interconnects' aspect ratio. For 90nm technologies, the ratio of an interconnects' parasitic coupling capacitance to its parasitic ground capacitance is nearly 5.5 (85% of the total parasitic capacitance) [1]. This signifies the increased dominance of coupling capacitances with technology scaling. It is there-

fore evident that the component of power dissipation corresponding to parasitic coupling capacitances is significant. In particular, on-chip bus has large parasitic coupling ones.

Power consumption estimation for coupling capacitances is more complicated than for ground capacitances. The power consumption for a parasitic coupling capacitance (termed coupling power) between two interconnects is dependent on the voltage difference across that capacitance. This in turn, is dependent on the relative switching activities of these interconnects. In addition to the dependence of coupling power on the relative switching activities of the coupled interconnects, the power consumed is dependent on the net's relative switching times [2]. The coupling power is dependent on the relative switching time difference. Relative delays, timing information, and switching activities are therefore, critical to accurate coupling power estimation.

In recent technologies, in addition to the coupling capacitance, the variability of circuit delay due to process, voltage and temperature variations (PVT variations) has become a significant concern. With increasing awareness of variations, a number of techniques are developed [3]~[5]. However, most of those focus on timing analysis. This means that only timing variations of critical path are considered. As previously described, relative delay due to these timing variations for tightly coupled interconnect lines cause also power consumption variation. The timing variation due to PVT variations is one of the sources of the relative delay variations. Another source is path delay variation. This variation also causes the temporal relative delay variation. These sources can be categorized into two types. We call those as chip specific (process dependent) and chip non-specific (condition dependent) variations. Chip specific variation means that each fabricated chip has a relative delay distribution due to process variation. The distribution of a chip is different from each other. Chip non-specific variation means that there is a relative delay distribution due to voltage/temperature variations and path delay variation in a chip. This distribution is same in all chips when application and environmental conditions are same. In this paper, we analyze only impact of process variations on the power consumption.

Objectives of our research are as follows: analyzing impact of the input relative delay variations on power consumption of a bus without and with low power bus coding techniques.

The remainder of the paper is organized as follows. In Section 2, along with some basic definitions, the power dissipation due to relative switching is described. In Section 3, power consumption of the bus when there are input arrival time variations is analyzed. Section 4 describes the experimental setup and presents the results. Section 5 concludes this paper.

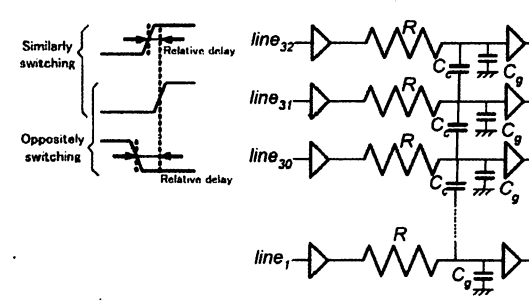

Figure 1 Capacitive coupled 32-bit bus structure ($N = 32$)

2. Power Model

2.1 Energy Model with Arrival Time Difference

Figure 1 shows a bus structure and input signal switchings with relative delays. Energy dissipation per cycle of a bus line E_d can be modeled as follows:

$$E_d = E_{dg} + E_{dc}$$
$$= \sum_{i=1}^{N} (\frac{1}{2} AF_i \cdot (C_g + \sum_{\text{all coupled line } j} MCF_{ij} \cdot C_c) \cdot V_{DD}^2).$$

where E_{dg} is the average dynamic energy dissipation due to self-switching of the line of interest, E_{dc} is the average dynamic energy dissipation due to relative switching between the line of interest and its adjacent lines. N is the bus width. AF_i is the activity factor of the line i and has a value of 0 when the line is quiet and 1 when the line is switching. MCF_{ij} is the Miller coupling factor value between the line of interest i and its adjacent coupled line j. The values of MCF are zero for similarly switching coupled lines, 1 when only one of the two coupled lines switches, and 2 when the coupled lines oppositely switch. C_g is the line-to-ground and load capacitance, C_c is the coupling capacitance between two neighboring lines and V_{DD} is the supply voltage. In addition to the dependence of coupling power on the relative switching activities of the coupled interconnects, the power consumed is dependent on the net's relative switching times. The coupling power is dependent on the relative switching time difference x. We analyze energy consumption due to relative switching with the delay. We assume ideal buffers (a buffer with even number of inverters), a line resistance R, a coupling capacitance C_c, a vertical capacitance component C_g, summation of these capacitance components C_t, and ideal step transitions.

Miller coupling factor MCF for energy modeling, in the presence of a relative delay, between adjacent lines can be written as [2]

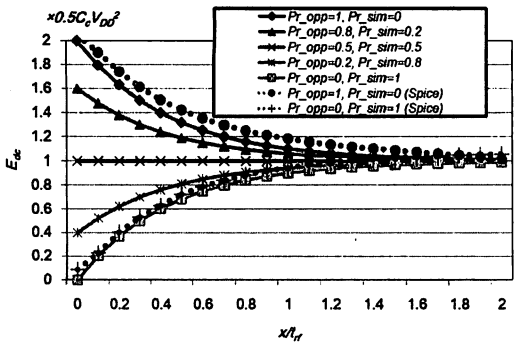

Figure 2 Energy dissipation varying the relative delay calculated by using equation (1)

$$MCF(x) = \begin{cases} 1, & \text{one-sided switching} \\ \left(1 + e^{\left(-\frac{2.3x}{t_{rf}}\right)}\right), & \text{oppositely switching} \\ \left(1 - e^{\left(-\frac{2.3x}{t_{rf}}\right)}\right), & \text{similarly switching} \end{cases} \quad (1)$$

where $t_{rf} = 2.3\tau(1+\gamma)$ is the 10-90% rise/fall time at the end of the line, $\tau = R \cdot C_t$, $\gamma = \frac{C_c}{C_t}$,

$$C_t = \begin{cases} C_c + C_g, & \text{outer bus lines} \\ 2C_c + C_g, & \text{inner bus lines.} \end{cases}$$

Figure 2 shows the energy dissipation associated with coupling capacitances with the relative delay. Note that the value of the capacitance ratio γ is 1, which is only coupling capacitances are assumed. Where Pr_opp and Pr_sim stand for the probabilities of occurrence of oppositely and similarly switchings between adjacent lines, respectively. In the figure, when $Pr\_opp + Pr\_sim = 1$ in the case having same delays, the energy dissipation $E_{dc}(d) = 0.5 \cdot C_C \cdot V_{DD}^2 \cdot \left(Pr\_opp \cdot \left(1 + e^{\left(-\frac{\pi}{\tau(1+\gamma)}\right)}\right) + Pr\_sim \cdot \left(1 - e^{\left(-\frac{\pi}{\tau(1+\gamma)}\right)}\right)\right)$ is shown. Dashed lines mean that the data is obtained by Spice simulation, which is transistor level simulation. The Spice used is Hspice from Synopsys Corp. The data includes short-circuit energy, but does not include leakage energy. Average error of the equation is about 6%. From the figure, this equation has good accuracy when changing the relative delay. This figure gives suggestions that unbalanced occurrence probability of oppositely (or similarly) switching is sensitive to the relative delay. On the other hand, well balanced occurrence of the switchings ($Pr\_opp + Pr\_sim = 0.5$) is free of the influence of the relative delay.

2.2 Power Model with Time Difference Distribution

We will now model power consumption of an N-bit bus. We assume that physical parameters of each wire such as wire length, height, width and pitch are same. The average power consumption of an N-bit bus P_d per clock cycle is given by:

$$P_d = P_{dg} + P_{dc},$$

$$P_{dg} = 0.5 \cdot C_g \cdot V_{DD}^2 \sum_{i=1}^{N} \alpha_i,$$

where P_{dg} denotes the dynamic power consumption corresponding to ground capacitance C_g, P_{dc} denotes the dynamic power consumption corresponding to coupling capacitance C_c, and α_i denotes switching (transition) probability at a bus line i. P_{dc} is given by

$$\sum_{i=1}^{N} \sum_{\text{all coupled line } j} P_{dc_{ij}}.$$

For a single coupled line with coupling capacitance C_c,

$$P_{dc} = P_{one} + P_{opp} + P_{sim},$$

where, P_{one}, P_{opp} and P_{sim} denote the coupling power when the coupled neighbor is not switching, switching in the opposite direction and switching in the same direction, respectively. We define single line switching (victim line switching) probability as Pr_one. P_{one} is time independent, while P_{opp} and P_{sim} are time dependent [6], that is, they depend on the relative switching times on the coupled two nets. P_{one} is expressed as

$$P_{one} = 0.5 \cdot C_c \cdot V_{DD}^2 \cdot Pr\_one.$$

P_{opp} is expressed as

$$P_{opp} = 0.5 \cdot C_c \cdot V_{DD}^2 \cdot \int_{-\infty}^{\infty} MCF_{opp}(x) \cdot p_{r_{opp}}(x) dx,$$

where, $p_{r_{opp}}(x)$ denotes the probability density that the nets switch in the opposite direction with a delay x. $p_{r_{opp}}(x)$ is used for representing relative delay variations in the following subsection, and $\int_{-\infty}^{\infty} p_{r_{opp}}(x)dx = Pr\_opp$. $MCF_{opp}(x)$ denotes an effective power factor as a function of the delay x for oppositely switching. A similar approach is employed for the computation of P_{sim}. P_{sim} is expressed as

$$P_{sim} = 0.5 \cdot C_c \cdot V_{DD}^2 \cdot \int_{-\infty}^{\infty} MCF_{sim}(x) \cdot p_{r_{sim}}(x) dx,$$

where, $p_{r_{sim}}(x)$ denotes the probability density that the nets switch in the same direction with a delay x. And, $\int_{-\infty}^{\infty} p_{r_{sim}}(x)dx = Pr\_sim$. $MCF_{sim}(x)$ denotes an effective power factor as a function of the delay x for similarly switching. x can be defined as $\mid d_i - d_j \mid$ where d_i and d_j are delays of bit line i and j, respectively.

3. Power Analysis Considering Signal Transition Types and Arrival Time Variations

When there is a complex equation for solving mathematically, the power consumption can be estimated by using

Monte Carlo simulation [7]. The total average power of the circuit is statistically estimated by simulating the circuit for randomly generated parameters. The power value is updated iteratively until it converges to the true power with a user-specified accuracy. In this paper, we analyze the power consumption of the bus with Molte Carlo simulation.

Assume that now we deal with only a pair of neighboring lines for power analysys.

$$\begin{aligned} P_d &= 0.5 \cdot f \cdot V_{DD}^2 \cdot (\alpha \cdot C_g + Pr\_one \cdot C_c \\ &\quad + \int_{-\infty}^{\infty} MCF_{opp}(x) \cdot p_{r_{opp}}(x)dx \cdot C_c \\ &\quad + \int_{-\infty}^{\infty} MCF_{sim}(x) \cdot p_{r_{sim}}(x)dx \cdot C_c) \\ &= 0.5 \cdot f \cdot V_{DD}^2 \cdot (\alpha \cdot C_g + (Pr\_one \\ &\quad + \int_{-\infty}^{\infty} MCF_{opp}(x) \cdot p_{r_{opp}}(x)dx \\ &\quad + \int_{-\infty}^{\infty} MCF_{sim}(x) \cdot p_{r_{sim}}(x)dx) \cdot C_c), \end{aligned}$$

where α denotes switching (transition) probability and $Pr\_one + Pr\_opp + Pr\_sim = \alpha$. The delay distributions for both $p_{r_{opp}}(x)$ and $p_{r_{sim}}(x)$ are normal distributions whose mean and variance are μ and σ, respectively. Here we focus only integral terms, which is defined as $f(x)$,

$$\begin{aligned} f(x) &= \int_{-\infty}^{\infty} MCF_{opp}(x) \cdot p_{r_{opp}}(x)dx \\ &\quad + \int_{-\infty}^{\infty} MCF_{sim}(x) \cdot p_{r_{sim}}(x)dx. \end{aligned}$$

Since $MCF_{sim}(x) = 2 - MCF_{opp}(x)$ from equation (1), we have

$$\begin{aligned} f(x) &= \int_{-\infty}^{\infty} MCF_{opp}(x) \cdot p_{r_{opp}}(x)dx \\ &\quad + \int_{-\infty}^{\infty} MCF_{sim}(x) \cdot p_{r_{sim}}(x)dx \\ &= \int_{-\infty}^{\infty} MCF_{opp}(x) \cdot p_{r_{opp}}(x)dx + 2 \cdot \int_{-\infty}^{\infty} p_{r_{sim}}(x)dx \\ &\quad - \int_{-\infty}^{\infty} MCF_{opp}(x) \cdot p_{r_{sim}}(x)dx \\ &= \int_{-\infty}^{\infty} MCF_{opp}(x) \cdot (p_{r_{opp}}(x) - p_{r_{sim}}(x))dx \\ &\quad +2Pr\_sim, \\ &\quad \text{because} \int_{-\infty}^{\infty} p_{r_{sim}}(x)dx = Pr\_sim. \end{aligned}$$

Since $MCF_{opp}(x) = 1 + e^{\left(-\frac{|x|}{\tau(1+\gamma)}\right)}$, $p_{r_{opp}}(x) = Pr\_opp \cdot \frac{1}{\sqrt{2\pi}\cdot\sigma} \cdot e^{\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)}$ and $p_{r_{sim}}(x) = Pr\_sim \cdot \frac{1}{\sqrt{2\pi}\cdot\sigma} \cdot e^{\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)}$, $\int_{-\infty}^{\infty} MCF_{opp}(x) \cdot (p_{r_{opp}}(x) - p_{r_{sim}}(x))dx$ can be written as

$$(Pr\_opp - Pr\_sim) \int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi}\cdot\sigma} \cdot e^{\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} \cdot \left(1 + e^{\left(-\frac{|x|}{\tau(1+\gamma)}\right)}\right) dx$$

$$\begin{aligned} &= (Pr\_opp - Pr\_sim)(\tfrac{1}{\sqrt{2\pi}\cdot\sigma} \int_{-\infty}^{\infty} e^{\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} dx \\ &\quad + \tfrac{1}{\sqrt{2\pi}\cdot\sigma} \int_{-\infty}^{\infty} e^{\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} \cdot e^{\left(-\frac{|x|}{\tau(1+\gamma)}\right)} dx) \\ &= (Pr\_opp - Pr\_sim)(1 \\ &\quad + \tfrac{1}{\sqrt{2\pi}\cdot\sigma} \int_{-\infty}^{\infty} e^{\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} \cdot e^{\left(-\frac{|x|}{\tau(1+\gamma)}\right)} dx), \\ &\quad \text{because} \tfrac{1}{\sqrt{2\pi}\cdot\sigma} \int_{-\infty}^{\infty} e^{\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} dx = 1. \end{aligned}$$

Here we only focus on terms depending the relative delay x, which is defined as follows:

$$g(x) = \frac{1}{\sqrt{2\pi}\cdot\sigma} \int_{-\infty}^{\infty} e^{\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} \cdot e^{\left(-\frac{|x|}{\tau(1+\gamma)}\right)} dx.$$

As a result, we have

$$\begin{aligned} P_d &= 0.5 \cdot f \cdot V_{DD}^2 \cdot (\alpha \cdot C_g + (Pr\_one + Pr\_opp + Pr\_sim \\ &\quad +(Pr\_opp - Pr\_sim) \cdot g(x)) \cdot C_c). \end{aligned}$$

Obviously, when the probabilities of oppositely and similarly switchings between adjacent lines are almost same, that is $Pr\_opp \simeq Pr\_sim$, the relative delay between the lines has little impace on power consumption. This is also a conclusion from the previous discussion in Figure 2. In other words, the relative delay affects power consumption in the case of unbalanced values between Pr_opp and Pr_sim. This is an important fact.

4. Experimental Results

In this work, we used a 32-bit global data bus structure shown in Figure 1 to conduct our simulations. We assume that all drivers (receivers) have uniform size and all signal wires have uniform width, spacing, and length. As a result, each bus line has same resistance R, ground capacitance C_g and coupling capacitance C_c. Interconnect technology parameters of 90nm process technology (C_g(fF/mm) is 47, C_c(fF/mm) is 72) are derived from [8]. Note that the most and least significant bus lines have coupling C_c. However, since the inner bus lines are sandwiched between two adjacent bus lines, the coupling is $2C_c$. Fixed parameters we used are as follows: wire length is 5mm, f is 100MHz, V_{DD} is 1V. The architectural simulators used in this study for a real application experiment are derived from the SimpleScalar/ARM version 2.0 tool set [9], a suite of functional and timing simulation tools for the ARM ISA. The selected application is the MPEG2 program with a 116k data.

For Monte Carlo simulation, to generate random number is needed. We used a uniform random number generator M-sequence [10], which is fast and has good randomness. The

period of sequence we used is 6.86×10^{156}.

Experimental results are shown in Table 1, 2 and. 3 The number of iterations for process dependent Monte Carlo simulation is 10. The number of input vectors is 100. We used 0ps and 1000ps as 3 sigma values of the process dependent relative delays. We assume that mean values of the delays are 0.

Table 1 shows experimental results for comparing Spice simulator with the Eq.(1) using Monte Carlo method for random input vectors. In the beginning, random input vectors as input for the bus are used. In other words, the input data is spatially and temporally uncorrelated with "0" and "1" being equiprobable. From the table, clearly we can find the fact that in the case of random vectors the relative delay variations do not affect the power consumption.

Table 2 shows experimental results for real input vectors, which is an mpeg2play program with a 116k bye image data. From this table, we can see an interesting fact: as increasing the variations of the relative delay, the average power consumption is larger (more than 10% of power consumption in the case of the non-variation situation).

Table 3 shows power consumption of the bus with/without low power bus coding technique (Bus Invert Coding [11]). In the Bus Invert Coding, if the Hamming distance between the present data and the last data of the bus is larger than $N/2$, the present data is transmitted with each bus inverted. In the case of real input vectors, power saving improved when there are variations. This is due to reduction of similarly switching with the coding. In the data stream, there are large amount of similarly switching due to sign extensions. Since these coding techniques reduce not only self switching but also similarly switching, power consumption of the bus with these coding whether there are variations or not.

Table 1 Power estimation results for random input vectors ($10^{-4}W$)

3 sigma of process var. (ps)	Spice	Eq. (1)
0	8.063	7.555
1000	8.059	7.540

Table 2 Power estimation results for real input vectors ($10^{-4}W$) (App.: mpeg2play)

3 sigma of process var. (ps)	Spice	Eq. (1)
0	3.550	3.225
1000	3.815	3.658

Table 3 Power estimation results for comparing low power bus coding with Eq. (1) ($10^{-4}W$) (App.: mpeg2play)

3 sigma of process var. (ps)	Uncoded	Bus Invert
0	3.330	3.062
1000	3.749	3.209

5. Conclusions

We have shown results of bus power analysis in the presence of input arrival time variations. The impact of variations on power consumption cannot be ignored. However, if we use variation tolerant low power coding such as the Bus Invert coding, the impact on power consumption becomes smaller. In other words, after analyzing main cause of power variation, to apply an appropriate bus coding for suppress the cause (oppositely or similarly switching) can reduce power variation. With advancing technology process, a large variety of variations has been turning up. Nondeterministic parameters considering the variability must be a new concern about not only delay estimation and leakage power estimation but also dynamic power estimation.

Acknowledgements 本研究は株式会社東芝および東京大学大規模集積システム設計教育研究センターを通し，(株) 半導体理工学研究センター，富士通 (株)，NEC エレクトロニクス (株)，(株) 東芝，(株) ルネサステクノロジ，シノプシス (株) の協力で行われたものである．貴重なご意見を頂いた福岡大学の佐藤寿倫教授および九州大学の松永裕介准教授に感謝いたします．本研究の一部は JST CREST-ULP によるものである．

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