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DSM配線とスーパーコネクトへの期待

桜井 貴康

東京大学、国際・産学共同研究センター
〒153-8505 東京都目黒区駒場 4-6-1
E-mail: tsakurai@iis.u-tokyo.ac.jp

あらまし今後の電子システムを考えるとシステムインパッケージやグローバルインテグレーションの重要性が増す。そこでは、数十μm といったデザインルールを有するスーパーコネクト技術が活躍する。このようなスーパーコネクト技術は VLSI が直面する IR ドロップや RC 遅延といった問題を解決するにも有効である。また、ディープサブミクロン配線の諸問題の解決を考えるとき、インダクタンスなどボードやパッケージでの設計知識が役立つ可能性がある。

キーワード VLSI、DSM、配線、スーパーコネクト

Deep Sub-Micron Interconnects and Expectation to Superconnect

Takayasu Sakurai

Center for Collaborative Research, and Institute of Industrial Science
University of Tokyo
4-6-1 Komaba, Meguro-ku, Tokyo, Japan, 153-8505
E-mail: tsakurai@iis.u-tokyo.ac.jp

Abstract Superconnect technology which is based on interconnections around 10um design rule is expected to realize new realm of electronic system integration together with System-on-a-Chip approaches. The superconnect technology will be helpful in solving deep submicron (DSM) interconnection issues of VLSI's such as IR voltage drop and RC delay problems. The accumulated knowledge database on board and package will be also useful in confronting DSM interconnection issues like inductive effects.

Key words VLSI, DSM, Interconnect, Superconnect

1. Abstract

Superconnect technology which is based on interconnections around 10μm design rule is expected to realize new realm of electronic system integration together with System-on-a-Chip approaches. The superconnect technology will be helpful in solving deep submicron (DSM) interconnection issues of VLSI's such as IR voltage drop and RC delay problems. The accumulated knowledge database on board and package will be also useful in confronting DSM interconnection issues like inductive effects.

2. Scaling and Issues of Current LSI Technology

Taking a close look at the scaling law, we can see that the following three crises are leaning over the LSI technology.

- Power crisis
- Interconnection crisis
- Complexity crisis

The power crisis is depicted in Fig.2. Lower operation voltage naturally increases operation current, which in turn requires thicker metal layers for the current to be distributed throughout the chip without IR-drop. One of the key approaches to low-power design is the memory embedding. By embedding memories, inter-chip communication power can be reduced by two orders of magnitude. The memory embedding, however, is an expensive option, since it increases process steps. A new system-level integration can be a solution to this problem.

As for the interconnection crisis, RC delay increase and IR-drop issue are some of the more stringent issues. Thicker metal layer used in an interposer/package/board may mitigate the problem.

Complexity crisis can only be solved by re-use of the pre-designed blocks and designing at higher abstraction level. Thus, System-on-a-Chip (SoC) where many pre-designed IP's are amalgamated at the higher abstraction is one of the candidates to cope with the complexity crisis. Future electronic systems, however, cannot be built only with the SoC, since many SoC issues have become evident as follows.

- Huge initial investment for masks & development
- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

The huge investment in developing the SoC process to embed different kinds of technologies is one of the most vital issues.

3. Superconnect

Recently, however, a new system-level integration called 'superconnect' is attracting attention[1-4], which may solve SoC problems. The superconnect connects separately built and tested chips not by printed circuit boards but rather directly to construct high-performance yet low-cost electronic systems. The superconnect may use around 10 micron level design rules [4]. Sometimes LSI's in the superconnect are connected in three-dimensional fashion to achieve the higher performance and the smaller geometry. System-in-a-Package (SiP) composed of stacked chips using bonding or interposers is one realization of the superconnect. The superconnect mitigate IR-drop problems and RC delay problems.

There has been a large gap between on-chip and off-chip interconnects in terms of power, density, performance, cost and turn-around-time. Basically, the large gap comes from the big difference between the design rules of on-chip and off-chip interconnects. It can be said that there is a technology vacuum at present between 1μm level on-chip interconnect and 100μm level off-chip interconnect. The superconnect will fill the gap between on-chip and off-chip interconnect, making use of 10μm level design rule.

Some of the important issues in the future system-level integration are as follows.

- Special design tools for placement & route for co-design of LSI's and assembly
- High-density reliable substrate and metallization technology
- low-cost, available known good die (reworkablility and module testing)

4. Issues in Deep Sub-Micron (DSM) Interconnects

The issues for DSM interconnects are summarized as follows:

Larger current
  IR drop (static and dynamic)
  Reliability (electro-migration)
Smaller geometry / Denser pattern
  RC delay

Signal Integrity
Crosstalk noise
Delay fluctuation
Higher speed
Inductance
EMI

Among others, IR drop and RC delay problems can have help from the superconnect technology. To fully utilize the merit of the thick metal layers of superconnect, co-design of VLSI and assembly will be necessary. As for inductive effects which appear in low resistance interconnects in VLSI's such as clock lines, power lines and wide buses, the knowledge accumulated in board and package designs will be transferred to VLSI community.

References

[1] T.Sakurai, "Superconnect Technology," Trans. C of IEICE, May 2001.

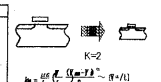
[2] M.Koyanagi et al., "Neuromorphic Vision Chip Fabricated Using Three-Dimensional Integration Technology," ISSCC Digest of Tech. Papers, pp.270-271, Feb.2001.

[3] K.Ohsawa, H.Odaira, M.Ohsawa, S.Hirade, T.Iijima, S.G.Pierce, "3-D Assembly Interposer Technology for Next-Generation Integrated Systems," ISSCC Digest of Tech. Papers, pp.272-273, Feb.2001.

[4] M.Kimura, "Superconnect: 21st Century LSI Production and Design Method", Nikkei Microdevices, no.180, pp.62-79, June 2000.

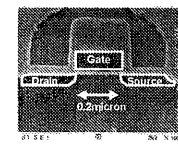
Scaling Law

Transistors		Scaling coefficients
V_{cc}	[V]	1/k
Tr. dimensions	[k]	1/k
Drain current	[I~1/k x/k V^1.3]	$1/k^{1.3}$
Gate capacitance	[C~1/k xx]	1/k
Tr. delay	[d~CV/I]	$1/k^{1.3}$
Tr. power	[P~VI~CV/d]	$1/k^{2.3}$
Power density	[p~P/a/a]	k
Tr. density	[n~1/a/a]	k^2
Interconnects		
Type / Scaling scenario		Local: Scaled; Global: Anti-scaled
Line thickness	[T]	1/k / k
Width	[W]	1/k / k
Separation	[S]	1/k / k
Oxide thickness	[H]	1/k / 1
Length	[L]	1/k / 1
Resistance	[R_{int}~L/W/T]	k / $1/k^2$
Capacitance	[C_{int}~LW/H]	1/k / k
RC delay/Tr. delay	[D~$R_{int}C_{int}$/d]	k^2 / –
Current density	[J~pWL/V /W/T]	– / k^2
DC noise / V_{cc}	[N~J/WT/R/V]	– / k^2



T.Sakurai&A.Newton,"Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas",IEEE JSSC, vol25, no.2, pp.584-594, Apr. 1990.

Scaling Law



Size 1/2

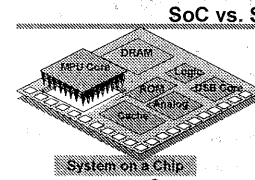
Favorable effects	
Size	x1/2
Voltage	x1/2
Electric Field	x1
Speed	x3
Cost	x1/4

Unfavorable effects	
Power density	x1.6
RC delay/Tr. delay	x3.2
Current density	x1.6
Voltage noise	x3.2
Design complexity	x4

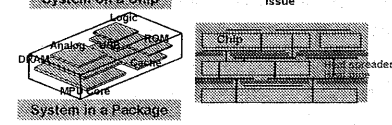
Issues in System-on-Chip

- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- Low yield due to larger die size
- Huge initial investment for masks & development
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

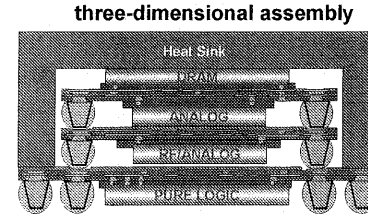
SoC vs. SiP



- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS...)
- Good electrical isolation
- Through-chip via
- Heat dissipation is an issue



Superconnect example based on three-dimensional assembly

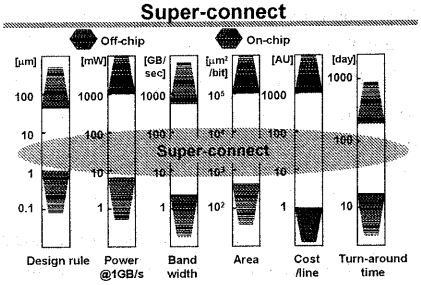


K.Ohsawa, H.Odaira, M.Ohsawa, S.Hirade, T.Iijima, S.G.Pierce, "3-D Assembly Interposer Technology for Next-Generation Integrated Systems," ISSCC Digest of Tech. Papers, pp.272-273, Feb.2001.

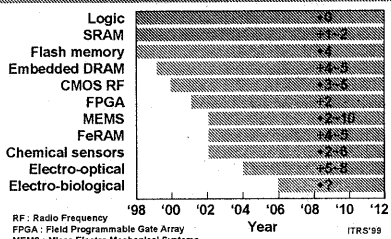
Issues in superconnect

- Special design tools for placement & route for co-design of LSI's and assembly
- High-density reliable substrate and metallization technology
- Low-cost, available known good die (reworkablility and module testing)

Super-connect



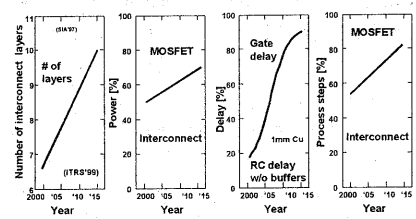
Technologies integrated on a chip



RF : Radio Frequency
FPGA : Field Programmable Gate Array
MEMS : Micro Electro Mechanical Systems
FeRAM : Ferroelectric RAM

Interconnect determines cost & perf.

P: Power, D: Delay, A: Area, T:Turn-around



New system level integration

- SoC : High-performance but issues remain
- Printed circuit board (PCB) : Low-performance

- New system level integration : Superconnect
  - Connects separately built and tested chips not by the PCB but rather directly to construct high-performance yet low-cost electronic systems
  - May use around 10 micron level design rules

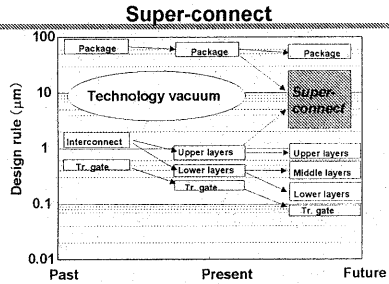
DSM interconnect design issues

Larger current
- IR drop (static and dynamic)
- Reliability (electro-migration)

Smaller geometry / Denser pattern
- RC delay
- Signal Integrity
- Crosstalk noise
- Delay fluctuation

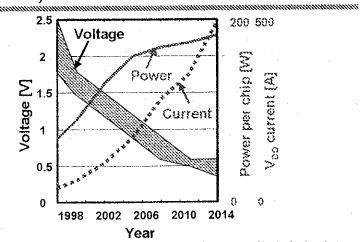
Higher speed
- Inductance
- EMI

Super-connect



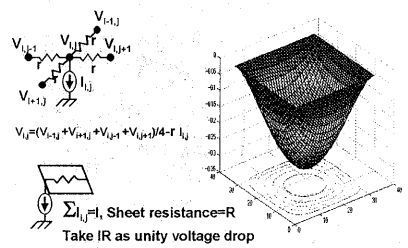
Nikkei microdevices

VDD, Power and Current Trend

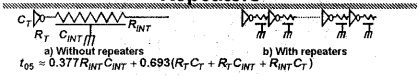


International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA), Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

IR Drop



Repeaters



$t_{05} \approx 0.377 R_{INT} C_{INT} + 0.693(R_T C_T + R_T C_{INT} + R_{INT} C_T)$

C_0 : Gate capacitance of minimum MOSFET

R_0 : Gate effective resistance of minimum MOSFET

$$Delay \approx k\left[p_1 \frac{R_{INT}}{k}\frac{C_{INT}}{k} + p_2\left(\frac{R_0}{h}hC_0 + \frac{R_0}{h}\frac{C_{INT}}{k} + \frac{R_{INT}}{k}hC_0\right)\right]$$: Buffered

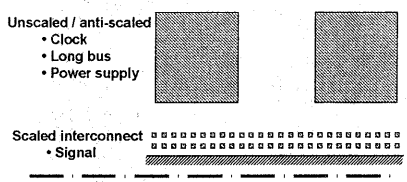
$$\frac{\partial Delay}{\partial h} = 0 \rightarrow h_{OPT} = \sqrt{\frac{C_{INT}R_0}{R_{INT}C_0}}$$: Optimized size of buffer inverter

$$\frac{\partial Delay}{\partial k} = 0 \rightarrow k_{OPT} = \sqrt{\frac{p_1}{p_2}\sqrt{\frac{R_{INT}C_{INT}}{R_0C_0}}}$$: Optimized number of stages

$$Delay_{OPT} = 2\left(\sqrt{p_1 p_2} + p_2\right)\sqrt{R_{INT}C_{INT}R_0C_0} \approx 2.4\sqrt{\tau_{INT}\tau_{MOS}}$$

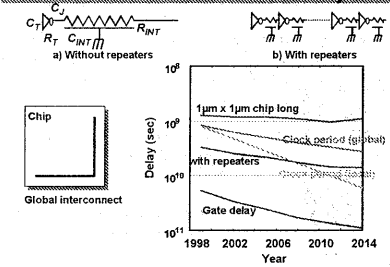
$$Cap.\ of\ gates = k_{OPT}h_{OPT}C_0 = \sqrt{p_1/p_2}\,C_{INT} \approx 0.73C_{INT}$$

Interconnect Cross-Section and Noise

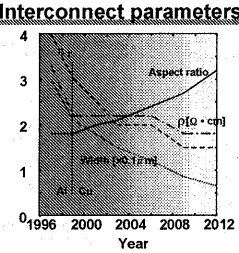


1V 20W → 20A current
2% noise on VDD & VSS → ~0.02V / 20A → ~10μm thick Cu
Thick layer interconnect, area pad, package are co-designed.

Buffered interconnect delay

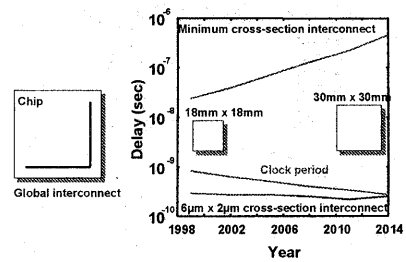


Interconnect parameters trend

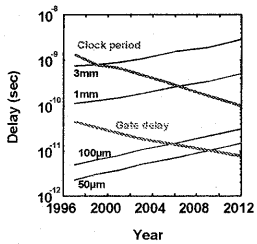


Semiconductor Industry Association roadmap
http://notes.sematech.org/1997pub.htm

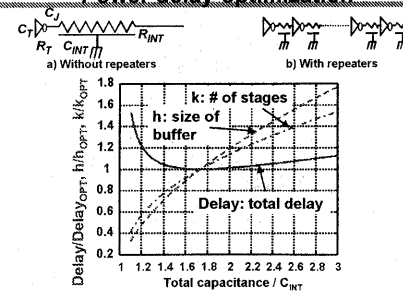
RC delay of global interconnections



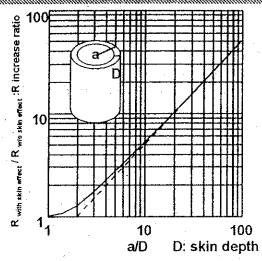
RC delay and gate delay



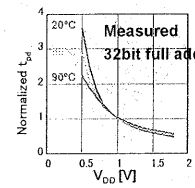
Power delay optimization

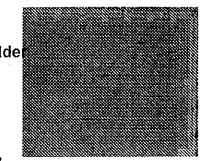


Skin Depth and R Increase



Reverse temperature dependence

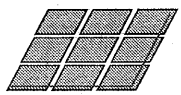




Photograph of 32bit FA
0.3μm CMOS

K.Kanda, K.Nose, H.Kawaguchi, and T.Sakurai,"Design Impact of Positive Temperature Dependence of Drain Current in Sub 1V CMOS VLSI's",CICC99, pp.563-566, May 1999.

Shorter interconnect in 3-D assembly



System on a chip

$$\frac{\#\ of\ devices\ in\ d\,(3D)}{\#\ of\ devices\ in\ d\,(2D)} = \frac{1}{3}\left(2\frac{d}{h}+\frac{h}{d}\right)$$
$$\approx \frac{2}{3}\left(\#\ of\ stacked\ chips\ in\ d\right)$$

d: Manhattan distance

h: Height between chips

3-D assembly

LSI in 2014

Year	Unit	1999	2014	Factor
Design rule		0.18	0.035	5.1
Tr. Density	/cm2	6.2M	390M	30
Chip size	mm2	340	900	2.6
Tr. Count per chip ( )		21M	3.6G	170
DRAM capacity		1G	1T	1000
Local clock on a chip	Hz	1.2G	17G	14
Global clock on a chip	Hz	1.2G	3.7G	3.1
Power	W	90	183	2.0
Supply voltage	V	1.5	0.37	0.2
Current	A	60	494.6	8
Interconnection levels		6	10	1.7
Mask count		22	28	1.3
Cost / tr. (packaged)	cents	1735	22	0.01
Chip to board clock	Hz	500M	1.5G	3.0
# of package pins		810	2700	3.3
Package cost	cents/pin	1.61	0.75	0.5

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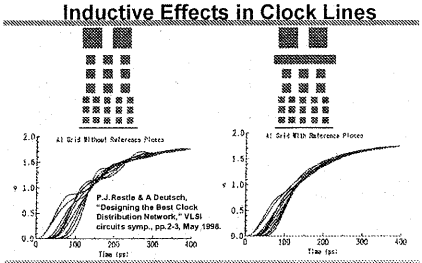
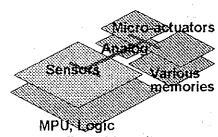
Inductive Effects in Clock Lines



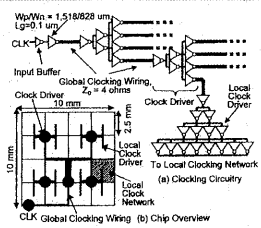
Board design practice is imported in LSI.

Possible electronic system in 2014



- Sensors/actutors
- 0.035μm 3.6G Si FET's with VTH & VDD control
- Locally synchronous 17GHz clock, globally asynchronous
- Chip / Package / Board system co-design for power lines, clocks, and long wires (super-connect)

H-tree clock distribution



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