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Evaluation of Microprocessors Placed-and-Routed with CNFET

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Abstract: CNFET (Carbon Nanotube Field Effect Transistor), which uses carbon nanotubes as transistor channels, is the next-generation MOSFET device and has a great potential in both improving the performance and reducing the power consumption of microprocessors. Due to high-speed switching and low power consumption, CNFET is expected to allow processor architects to adopt new microarchitecture in processor design; however, the nature of microprocessors implemented with CNFET (a.k.a., CNFET processors) is little known. In particular, performance, power consumption, and area of individual units within microprocessors placed-and-routed with CNFET have not been reported yet. In this paper, we show performance, power consumption, and area of two microprocessors (i.e., RSD and OpenSPARC T2) placed-and-routed with CNFET5 and CNFET7 technologies while comparing the experimental results with ASAP7, FreePDK15, and FreePDK45. Our experimental results show that processor units with CNFET7 consume up to 94.5% and 94.6% smaller power than those with ASAP7 at a frequency of 0.8 GHz in RSD and OpenSPARC T2 , respectively, in exchange for 2x area overheads, and CNFET5 that has the same area overhead as CNFET7 shows further reduction in power consumption when compared to CNFET7.

Keywords: CNFET, Place and Route, OpenSPARC T2, RSD

1. Introduction

As we reach the end of Moore's law [4], new materials and devices are explored to improve the performance of LSI [8]. Although various next-generation devices such as spin MOSFET [17] and tunneling FET [10] have been being developed, CNFET (Carbon Nanotube Field Effect Transistor) is one of the promising alternative devices to silicon MOSFET [20]. CNFET uses nanometer-order carbon nanotubes as transistor channels and enables high-speed switching with low voltage [21]. As an example of the great potential of CNFET, it is reported that 10-nm CNFET shows 3.9x and 9.4x improvements in gate delay and energy efficiency, respectively, when compared to 10-nm FinFET [15].

This attractive nature drives some researchers to implement microprocessors with CNFET, which are called CNFET processors. For example, Hill et al. placed and routed an inorder processor with 5nm and 7nm CNFET technologies and showed that the resulting processors operated at 3x higher clock frequency with one third energy savings than processors made by FinFET [6]. They also created a test chip of another inorder processor with 7nm CNFET technology and reported that the test chip succeeded in operation at 10 KHz [7]. These studies show the great potential of CNFET processors, but do not provide sufficient insight into the design of CNFET-aware microarchitecture because they do not show performance, power, and area of individual units within CNFET processors. Furthermore, they focus on inorder processors and the impact of CNFET on out-of-order processors is therefore still unknown.

In this context, we have analyzed CNFET processors in more detail. For example, our previous report [24] provides a unit-level analysis on performance, power, and area of an inorder CNFET processor after logic synthesis while comparing a FinFET processor. We however have not performed a unit-level analysis on an inorder CNFET processor after place and route. In addition, analyzing the impact of CNFET on an out-of-order processor has been out of the scope.

In this paper, we place and route OpenSPARC T2 [22] with CNFET and then perform a unit-level analysis on performance, power, and area of the resulting processor. We also place and route RSD [12], which is an out-of-order RISC-V processor, and then show the impact of CNFET on various units needed for out-of-order execution.

The reminder of this paper is organized as follows. In Section 2, we describe several PDKs (Process Design Kits) we use for place and route. We explain our experimental methodology in Section 3, and our experimental results are shown in Section 4. Finally, we conclude this paper in Sec-

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Table 1: Layer configuration of ASAP7

Layer	Lithography	Pitch (nm)	Width (nm)
Fin	SAQP	27	6.5
$Active$	EUV	108	54
$Gate$	SADP	54	21
$SDT/LISD$	EUV	54	25
LIG	EUV	54	16
$VIA0-VIA3$	EUV	25	18
$M1-M3$	EUV	36	18
$M4, M5$	SADP	48	24
$VIA4, VIA5$	LELE	34	24
$M6, M7$	SADP	64	32
$VIA6, VI77$	LELE	45	32
$M8, M9$	SE	80	40
$VIA8$	SE	57	40

tion 5.

2. Process Design Kits

We use two types of open-source PDKs (i.e., FreePDK and ASAP7) for the design with silicon MOSFET, and one in-house PDK (i.e., CNFET PDK) for the design with CNFET.

2.1 FreePDK

FreePDK is a set of open-source PDKs maintained by North Carolina State University [13]. It includes two major PDKs. One is for logic design with a planar MOSFET manufactured with a 45nm technology node (a.k.a., FreePDK45), and the other is for logic design with FinFET manufactured with a 15nm technology node (a.k.a., FreePDK15). It is reported that FreePDK15 can reduce area and leakage and dynamic power consumption of a FPU by 89.7%, 60.3% and 60.2%, respectively, and improve slack of the FPU from 0ps to 307.5ps when compared to FreePDK45 [11]. Because FreePDK provides not only library files needed for logic synthesis but also LEF (Library Exchange Format) files used in a place-and-route process in the Cadence design flow, use of Cadence EDA tools is recommend in FreePDK.

2.2 ASAP7

ASAP7 is released as open source by Arizona State Univeristy [1]. It provides a predictive technology model of 7nm FinFET with an assumption of EUV (Extreme Ultraviolet Lithography), which is needed for sub-10nm patterning [3]. Table 1 summarizes the layer configuration of ASAP7. The use of EUV makes ASAP7 more practical when assessing the impact of the latest FinFET on circuit.

ASAP7 supports logic design with Cadence EDA tools officially. If we use the other tools such as Synopsys IC Compiler for logic design using ASAP7, a supplemental PDK is needed additionally [14].

We use the transistor model with SLVT (Super Low Threshold Voltage) and the TT (typical/typical) process corner for our experiment, though three threshold voltages (i.e., SLVT, LVT, RVT) and three process corners (i.e., SS, TT, FF) are available in ASAP7.

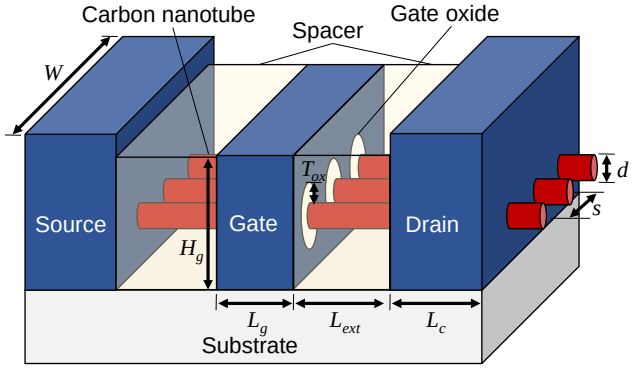

Fig. 1: VS-CNFET

2.3 CNFET PDK

To the best of our knowledge, there is no open-source PDK for logic design with CNFET, though some research groups report that CNFET PDKs are used for logic design [6], [7]. We therefore create new CNFET PDKs by combining fragmented information on CNFET PDKs with a few assumptions we newly introduce.

Our PDKs consist of two components that model the 5nm and 7nm CNFET technology nodes used in the literature [6]. We refer to the PDKs for the 5nm and 7nm technology nodes as CNFET5 and CNFET7, respectively.

In both PDKs, Stanford VS-CNFET [21] is used as a base transistor model. Figure 1 illustrates the structure of VS-CNFET. VS-CNFET is a cylindrical GAA (gate-all-around) MOSFET with several carbon nanotubes as the channel materials. A SPICE-compatible model is available for VS-CNFET. It is suitable for studies of sub-10nm CNFET technology nodes because it models various effects appeared in sub-10nm technology nodes such as tunneling leakage current precisely.

We use VS-CNFET and specific values of transistor parameters to mimic the 5nm and 7nm CNFET models used in the previous work. The values of the main parameters (e.g., gate width) in the 5nm and 7nm CNFETs are shown in the literature [6] but some parameter values are not; we therefore search the missing values using a parameter search method. The resulting CNFET models has an error of up to 2.7% in I-V characteristics. Thus, we well reproduce the CNFET models used in the previous work.

With these models, we generate the library files for CNFET5 and CNFET7. We create 56 SPICE netlists for the cells included in each library (e.g., INV_X1) and then compute both delay and power consumption of each cell by simulating the corresponding netlist with HSPICE. CCS (Composite Current Source) and NLDM (Non-Linear Delay Model) are used as the delay models. The area of each cell is calculated from the area of the corresponding cell in NanGate 15nm Open Cell Library [19] by using the scaling factor computed from the ratio of the gate pitches of two cells. This method is used also in the library generation tool [5] used in the previous work.

The layer configurations of CNFET5 and CNFET7 are

Table 2: Layer configuration of CNFET5

layer	Pitch (nm)	Width (nm)
Gate	42	/
Plug	42	/
$M0$	21	10.5
$M1$	21	12
$M2, M3$	21	12
$M4, M5$	48	24
$M6 - M8$	72	36
$V0 - V1$	21	12
$V12, V23$	21	12
$V34$ (V)	21	12
$V45$ (V)	48	24
$V56$ (V)	48	24
$V67, V78$ (V)	72	36

Table 3: Layer configuration of CNFET7

layer	Pitch (nm)	Width (nm)
Gate	42	/
Plug	42	/
$M0$	32	21
$M1$	42	24
$M2, M3$	32	16
$M4, M5$	48	24
$M6 - M8$	80	40
$V0, V1$	32	21
$V12, V23$	32	16
$V34$ (V)	40	16
$V45$ (V)	48	24
$V56$ (V)	64	24
$V67, V78$ (V)	80	40

shown in Tables 2 and 3, respectively. These configurations are the same as the layer configurations of the CNFET technology nodes used in the previous work [6]. We determine cell layout such as pin coordinates according to the scaling method used in cell area calculation. With these layer configurations and cell layout, we create the LEF files for CNFET5 and CNFET7.

We note that no macro (e.g., an SRAM macro) is included in CNFET5 and CNFET7. This is because macros are special logic highly tuned for a given technology node and much of experience and expertise are therefore needed to design macros. We will add some macros into CNFET5 and CNFET7 in the future.

3. Experimental Methodology

3.1 Microprocessors

We use two microprocessors (OpenSPARC T2 and RSD) for our experiment.

3.1.1 OpenSPARC T2

OpenSPARC T2 [22] is an open-source processor developed by Oracle. OpenSPARC T2 is a multi-core processor composed of eight in-order cores, as shown in Figure 2. Each core has 8-stage integer and 12-stage floating-point pipelines and processes up to eight threads in a fine-grained multithreading manner. The memory system consists of private L1 and shared L2 caches.

The main units within the core are listed below:

IFU (Instruction Fetch Unit) consists of the following three subunits.

CMU (Cache Miss Logic Unit) processes instructions that cause cache misses.

FTU (Fetch Unit) fetches instructions from the memory system.

IBU (Instruction Buffer Unit) stores the instructions fetched by FTU.

PKU (Pick Unit) selects a thread to be executed next from multiple executable threads.

DEC (Decode Unit) decodes instructions.

EXU (Execution Unit) performs integer arithmetic and logic operations except for multiplication and division. Two EXUs are installed in each core.

FGU (Floating-Point and Graphics Unit) performs floating-point arithmetic, image processing, and integer multiplication/division operations.

LSU (Load/Store Unit) executes load/store instructions.

MMU (Memory Management Unit) performs memory protection and address translation.

PMU (Power Management Unit) controls power consumption of units with clock gating.

TLU (Trap Logic Unit) handles exceptions and traps.

GKT (Gasket) arbitrates requests for a crossbar switch connecting cores and caches.

We focus on these 3+9 units and the other units within a core are not covered in this paper. This is because performing logic synthesis for the other units such as L1 caches and register files, which are called megacells [23], without SRAM macros is unrealistic. Our future work is to evaluate the impact of CNFET on megacells.

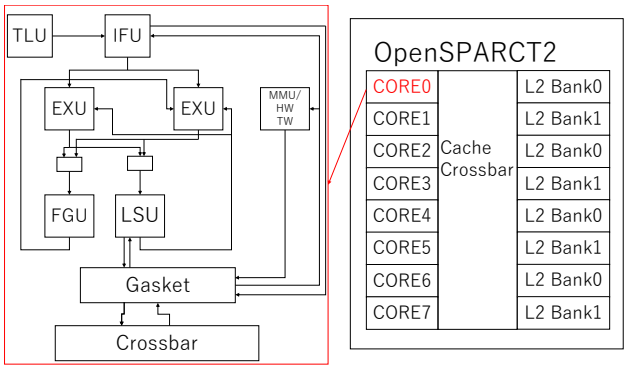

Fig. 2: OpenSPARC T2 microarchitecture

3.1.2 RSD

RSD, which is developed in collaborations with mainly Kyushu University and Tokyo University, is a 32-bit FPGA-optimized RISC-V out-of-order superscalar processor [12]. The front-end pipeline has 6 stages and fetches up to 2 instructions simultaneously. The back-end pipeline consists of 5-7 stages (depending on instructions) and issues up to 5 instructions per cycle. The source code of RSD is available at [18].

Figure 3 shows the micro architecture of RSD. We focus on the following components in this paper due to the limitation of our PDK, which is described in Section 2.3.

SCD (Scheduler) determines which instructions are issued next.

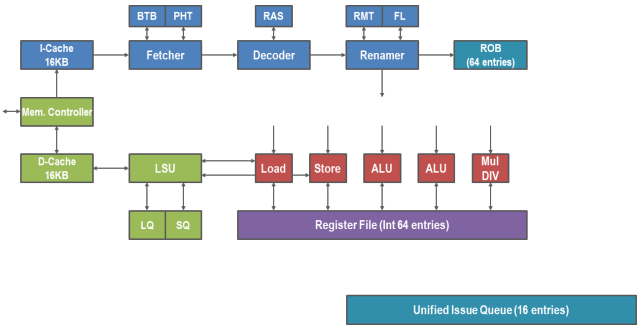

Fig. 3: RSD microarchitecture

Table 4: Timing constraints used for logic synthesis

Parameters	Values
Clock frequency	0.8Ghz
Max fanout	6
Clock transition	0.05
Waveform(Rise time:Fall time)	1:1

MDU (multiplier/divider Unit) executes multiplication and division operations.

PMU (Pipelined Multiplier Unit) executes multiplication operations in a pipelined manner.

PVA (Pipelined Vector Adder executes vector addition operations in a pipelined manner.

PVM (Pipelined Vector Multiplier) executes vector multiplication operations in a pipelined manner.

IOU (Input/Ouput Unit) executes I/O instructions.

CSRU (Control and Status Register Unit) manages control and status registers that store various information in the processor.

PC (Performance Counter) counts the number of hardware-related events in the processor.

PBC (Pipelined Bit Counter) counts the number of bits in a pipelined manner.

3.2 Design Flow

With 5 PDKs (FreePDK15, FreePDK45, ASAP7, CNFET5 and CNFET7), we evaluate the delay, power consumption, and area of the units included in OpenSPARC T2 and RSD cores after place-and-route. We use the Cadence EDA tools (i.e., Genus Synthesis Solution 18.13 and Innovus 19.17) for logic synthesis and place-and-route.

3.2.1 Logic Synthesis

Table 4 summarizes timing constraints we use for logic synthesis. In most cases (e.g., max fanout), we use the default values used in the scripts included in the code base of OpenSPARC T2. These scripts are written for Synopsys Design Compiler, but Genus can read SDC (Synopsys Desing Constraints) code. Because RSD does not support the design flow of hardware except for FPGA, we use the same values for RSD as those of OpenSPARC T2.

We use a frequency of 0.8 GHz as a target clock frequency because all processors satisfy it after logic synthesis; however, delay, power consumption, and area of synthesized circuit depend on target clock frequency. We will evaluate the delay, power consumption, and area of two processors at different clock frequencies in the future.

As for max transition, we use the value recommended by each PDK. The optimal value of max transition is written in a library file included in each PDK.

With these timing constraints, we perform logic synthesis for two processors with each PDK. After that, we can obtain some gate-level verilog netlist and SDC files. We use these files for place and route.

3.2.2 Place and Route

One problem in place and route is that Innovus provided for academic use does not allow to do place and route for sub-10nm technology nodes. An optional license, which is very expensive, is needed for place and route for such advanced technology nodes. Scaling up various information such as layout information is often used to avoid this problem, and the LEF and QRC files where various information is scaled by a factor of 4 is bundled in ASAP7 [3]. We use this approach also for CNFET5 and CNFET7.

The scaling approach, however, yields undesirable results when we evaluate the impact of an advanced technology node on a circuit. Because the scaling approach is not used in a real manufacturing process, place and route with the scaling approach may overestimate the delay, power consumption, and especially area of a given circuit.

In this paper, we try to adjust the delay, power consumption, and area obtained from place and route with the scaling approach. Our approach is as follows. First, we collect sample data (i.e., delay, power consumption, and area) of a given circuit under different scaling factors by performing place and route with multiple scaling factors. Second, with the above sample data and a curve fitting technique, we create per-parameter models to predict parameter values against scaling factors. More specifically, we use linear regression for prediction in delay and power consumption, while we use a quadratic function for area prediction. Finally, we extrapolate the delay, power consumption, and area of the circuit with these models in case that we do not use the scaling approach.

We validate our approach with FreePDK15 in case of prediction in power consumption and area. In contrast, our delay-prediction method may contain an error because we perform linear regression for the delay of the critical paths on a circuit, which are defined after place and route and therefore differ between scaling factors. When collecting sample data, we use the scaling factors of 2, 3 and 4 for both ASAP7 and CNFET7, while we use the scaling factors of 3, 4 and 6 for CNFET5.

We note that we apply the above approach only to the LEF file in each PDK because our PDKs have no QRC file. Since QRC files enable Innovus to produce more precise and realistic results, use of QRC files is preferable in a place-and-route process. Our future work is to create QRC files for our PDKs. We also note that our experimental results of ASAP7 take the effect of the QRC files into account.

Table 5: Total power consumption of OpenSPARC T2. The units of the numbers without parentheses are mW. The numbers within parentheses represent percentages against ASAP7.

Unit	CNFET5	CNFET7	ASAP7	FreePDK15
DEC	0.2(3.8)	0.4(6.1)	6.0	10.5(175.5)
EXU	28.6(31.1)	38.3(41.6)	92.0	243.1(264.3)
GKT	10.3(18.6)	10.8(19.5)	55.3	118.1(213.6)
IFU_CMU	18.0(32.9)	21.3(38.9)	54.8	115.4(210.5)
IFU_FTU	33.7(27.2)	37.2(30.0)	124.1	444.6(358.3)
IFU_IBU	50.8(39.2)	46.0(35.5)	129.5	326.9(252.5)
LSU	78.7(28.0)	99.9(35.6)	280.7	751.0(267.6)
PKU	0.7(4.4)	0.8(5.4)	15.8	32.7(207.0)
TLU	116.3(33.2)	145.2(41.5)	349.9	1021.0(291.8)
PMU	15.4(31.3)	16.3(33.1)	49.2	111.8(227.2)
FGU	269.6(37.5)	256.9(35.7)	718.8	1967.0(273.7)
MMU	77.2(30.9)	94.6(37.8)	250.0	754.4(301.8)

Table 6: Leakage power consumption of OpenSPARC T2. The units of the numbers without parentheses are mW. The numbers within parentheses represent percentages against ASAP7.

Unit	CNFET5	CNFET7	ASAP7	FreePDK15
DEC	0.0050(22.1)	0.008(35.4)	0.0226	0.0424(187.6)
EXU	0.0211(23.3)	0.034(38.0)	0.0906	0.1696(187.2)
GKT	0.0143(25.0)	0.0234(41.0)	0.0571	0.1192(208.8)
IFU_CMU	0.0105(22.5)	0.0175(37.6)	0.0466	0.0862(185.0)
IFU_FTU	0.0304(22.9)	0.0493(37.2)	0.1326	0.2565(193.4)
IFU_IBU	0.0341(24.7)	0.0573(41.6)	0.1378	0.2846(206.5)
LSU	0.0659(22.7)	0.107(36.8)	0.2905	0.5496(189.2)
PKU	0.0162(25.8)	0.0254(40.4)	0.0628	0.1365(217.4)
TLU	0.0852(23.6)	0.1375(38.0)	0.3616	0.7027(194.3)
PMU	0.0135(26.2)	0.0219(42.4)	0.0516	0.1075(208.3)
FGU	0.1085(25.0)	0.1735(39.9)	0.4343	0.7878(181.4)
MMU	0.0501(23.5)	0.0819(38.5)	0.2130	0.4091(192.1)

4. Experimental Results

4.1 OpenSPARC T2

Because we were unable to perform place and route for OpenSPARC T2 with FreePDK45 correctly, we will show the experimental results of the other PDKs.

4.1.1 Power Consumption

Table 5 shows the total power of the units in an OpenSPARC T2 core placed-and-routed with different PDKs. As shown in the table, FreePDK15 consumes about twice the power of ASAP7, while the CNFET7 can consume only about 35% of the power of ASAP7 on average. In particular, CNFET7 shows a reduction of 94.6% in total power for PKU when compared to ASAP7. CNFET5 can reduce the power of CNFET7 by about 20% additionally.

Table 6 shows the leakage power of the units in an OpenSPARC T2 core. As shown in the table, ASAP7 consumes about half of the leakage power of FreePDK15, while CNFET5 and CNFET7 can reduce the leakage power of ASAP7 greatly (by about 20% and 40% on average, respectively). Specifically, CNFET5 can reduce the leakage power of ASAP7 by up to 78.9% (DEC).

Table 7 shows the ratio of leakage power to total power in an OpenSPARC core. As shown in the table, many units show an almost identical percentage for four PDKs. It means that all PDKs affect the dynamic and static power of the units evenly. In contrast to this, CNFET5 and CNFET7 show larger percentage than ASAP7 and FreePDK15 for a few units (i.e., DEC, GKT and PKU). It means that CNFET5 and CNFET7 have more ability to reduce dynamic power than ASAP7 and FreePDK15 for these units.

Table 7: Ratio of leakage power consumption to total power consumption in OpenSPARC T2

Unit	CNFET5	CNFET7	ASAP7	FreePDK15
DEC	2.22	2.22	0.38	0.40
EXU	0.07	0.09	0.10	0.07
GKT	0.14	0.22	0.10	0.10
IFU_CMU	0.06	0.08	0.08	0.07
IFU_FTU	0.09	0.13	0.11	0.06
IFU_IBU	0.07	0.12	0.11	0.09
LSU	0.08	0.11	0.10	0.07
PKU	2.33	3.00	0.40	0.42
TLU	0.07	0.09	0.10	0.07
PMU	0.09	0.13	0.10	0.10
FGU	0.04	0.07	0.06	0.04
MMU	0.06	0.09	0.09	0.05

Table 8: Area of OpenSPARC T2. The units of the numbers without parentheses are μm^2. The numbers within parentheses represent percentages against ASAP7.

Unit	CNFET5	CNFET7	ASAP7	FreePDK15
DEC	513.0(171.1)	512.5(170.9)	299.9	1194.9(398.5)
EXU	2113.7(172.8)	2131.5(174.2)	1223.3	4749.9(388.3)
GKT	1537.1(181.5)	1548.5(182.9)	846.7	3425.2(404.5)
IFU_CMU	1084.1(166.3)	1097.0(168.2)	652.0	2376.3(364.4)
IFU_FTU	3164.4(171.7)	3169.5(172.0)	1843.0	7168.1(388.9)
IFU_IBU	3594.8(172.4)	3674.8(176.2)	2085.3	7915.8(379.6)
LSU	6767.2(173.7)	6789.7(174.3)	3895.8	15116.2(388.0)
PKU	1651.7(180.9)	1618.4(177.2)	913.2	3668.0(401.7)
TLU	8772.9(177.6)	8777.8(177.7)	4939.4	19592.6(396.7)
PMU	1407.4(188.4)	1412.3(189.0)	747.1	3055.0(408.9)
FGU	10804.3(178.4)	10820.9(178.7)	6057.0	22907.0(378.2)
MMU	5379.0(178.0)	5396.4(178.6)	3022.3	11874.7(392.9)

4.1.2 Area

The area of the units in an OpenSPARC T2 core is shown in Table 8. As shown in the table, the area of FreePDK15 is about 4x larger than that of ASAP7, while the area of CNFET5 and CNFET7 is about 1.7x larger than that of ASAP7. In contrast to this, CNFET5 and CNFET7 show little difference in area for every unit because each type of a cell in CNFET5 has the same area as that in CNFET7.

4.1.3 Delay

Table 9 shows the delay of the units in an OpenSPARC T2 core. Since FreePDK15 does not need the scaling approaches described in Section 3.2.2, we omit the experimental results of FreePDK15 from the table. Moreover, some units such as FGU are removed from the table because the timing paths of these units are not shown in the final timing reports.

The experimental results shown in the table look a little odd. Although CNFET5 and CNFET7 show smaller delay than ASAP7 for some units such as DEC, they show very larger delay than ASAP7 for the other units. This is because our delay prediction method described in Section 3.2.2 might be inaccurate. In our method, models generated by performing linear regression for critical path delay are used

Table 9: Delay of OpenSPARC T2. The units of the numbers without parentheses are ps. The numbers within parentheses represent percentages against ASAP7.

Unit	CNFET5	CNFET7	ASAP7	Path
DEC	468.6(66.3)	230.1(32.6)	706.3	i2o
EXU	354.9(203.5)	384.4(220.4)	174.4	i2o
GKT	26.8(34.7)	28.5(36.9)	77.2	i2o
IFU_CMU	316.6(141.6)	421.4(188.4)	223.6	i2o
IFU_FTU	571.7(529.3)	886.0(820.4)	108.0	i2o
LSU	167.2(143.0)	358.1(306.3)	116.9	i2o
PKU	250.7(38.9)	523.9(81.4)	644.0	i2o
TLU	132.6(13.4)	124.1(12.5)	992.0	i2o

Table 10: Total power consumption of RSD. The units of the numbers without parentheses are mW. The numbers within parentheses represent percentages against ASAP7.

Unit	CNFET5	CNFET7	ASAP7	FreePDK15	FreePDK45
CSRU	0.0324(7.6)	0.0399(9.4)	0.424	0.936(220.5)	2.222(523.5)
IOU	0.0118(7.0)	0.0145(8.6)	0.169	0.361(213.3)	0.972(574.0)
LSU	0.0187(18.8)	0.0219(22.0)	0.099	0.451(454.2)	1.062(1069.3)
MDU	0.3712(14.2)	0.5246(20.1)	2.614	7.388(282.6)	28.53(1091.3)
PC	0.0178(5.3)	0.0210(6.3)	0.334	0.556(166.6)	1.622(485.7)
PBC	0.0017(8.0)	0.0019(9.2)	0.021	0.035(170.7)	0.137(667.2)
PMU	0.3612(17.7)	0.4621(22.7)	2.037	6.346(311.5)	25.3(1241.8)
PVA	0.0352(4.9)	0.0395(5.5)	0.719	0.874(121.5)	2.709(376.9)
PVM	1.2608(19.1)	1.8430(27.9)	6.617	26.2(395.9)	90.5(1367.7)
SCD	0.0094(7.0)	0.0110(8.2)	0.134	0.271(201.6)	0.524(390.0)

for prediction, but possibly critical path delay has no linear relationship with scaling factors. It may be better to use non-linear functions to improve prediction accuracy.

4.2 RSD

4.2.1 Power Consumption

Table 10 shows the total power consumption of the units in an RSD core. We can see that CNFET7 can reduce the total power consumption by up to 94.5% (PVA) and at least 72.1% (PVM) when compared to ASAP7. In addition, CNFET5 can reduce the total power consumption by about 20% when compared to CNFET7.

Table 11 shows the leakage power of the units in an RSD core. As shown in the table, CNFET5 and CNFET7 can reduce the leakage power of the units largely when compared to the silicon MOSFET PDKs. For example, CNFET5 shows a reduction of up to 80.4% in leakage power when compared to ASAP7.

Table 12 shows the percentage of leakage power against total power for the units in an RSD core. As shown in the table, CNFET5 and CNFET7 show higher percentages of leakage power against total power consumption than the other PDKs. For example, PBC consumes 30.0% of the total power as leakage power for CNFET7, while it consumes 5.0% of the total power as leakage power for ASAP7. This means that CNFET5 and CNFET7 have more ability to save dynamic power. We note that ASAP7 shows a bit higher percentages than FreePDK; i.e., the percentage of leakage power of circuit increases as technology nodes advance. It is the well-known trend of silicon MOSFET scaling and shown also in the literature [16].

Table 11: Leakage power consumption of RSD. The units of the numbers without parentheses are mW. The numbers within parentheses represent percentages against ASAP7.

Unit	CNFET5	CNFET 7	ASAP7	FreePDK15	FreePDK45
CSRU	0.0031(26.3)	0.0052(44.1)	0.0117	0.0266(227.5)	0.0131(111.6)
IOU	0.0016(29.6)	0.0026(46.4)	0.0055	0.0132(240.5)	0.0066(119.5)
LSU	0.0014(22.0)	0.0023(36.4)	0.0062	0.0118(189.2)	0.0063(100.3)
MDU	0.0096(21.9)	0.0170(38.7)	0.0438	0.0680(155.4)	0.1441(329.4)
PC	0.0024(25.6)	0.0037(39.5)	0.0093	0.0187(200.9)	0.0073(78.5)
PBC	0.0004(39.4)	0.0006(55.0)	0.0010	0.0020(191.3)	0.0025(241.2)
PMU	0.0063(19.8)	0.0119(36.9)	0.0321	0.0426(132.7)	0.1258(392.2)
PVA	0.0030(23.3)	0.0048(38.0)	0.0127	0.0160(125.4)	0.0111(87.0)
PVM	0.0254(19.6)	0.0474(36.6)	0.1297	0.1703(131.4)	0.4258(328.4)
SCD	0.0011(25.4)	0.0018(41.1)	0.0043	0.0097(224.0)	0.0051(118.5)

Table 12: Ratio of leakage power consumption to total power consumption in RSD

Unit	CNFET5	CNFET7	ASAP7	FreePDK15	FreePDK45
CSRU	9.5	12.9	2.8	2.8	0.6
IOU	13.8	17.6	3.2	3.7	0.7
LSU	7.4	10.4	6.3	2.6	0.6
MDU	2.6	3.2	1.7	0.9	0.5
PC	13.4	17.5	2.8	3.4	0.4
PBC	24.6	29.9	5.0	5.6	1.8
PMU	1.8	2.6	1.6	0.7	0.5
PVA	8.4	12.3	1.8	1.8	0.4
PVM	2.0	2.6	2.0	0.7	0.5
SCD	11.8	16.2	3.2	3.6	1.0

Table 13: Area of RSD. The units of the numbers without parentheses are μm^2. The numbers within parentheses represent percentages against ASAP7.

Unit	CNFET5	CNFET7	ASAP7	FreePDK15	FreePDK45
CSRU	332(193)	331(192)	172	751(437)	2840(1652)
IOU	167(205)	165(202)	82	357(437)	1464(1792)
LSU	146(170)	146(170)	86	330(385)	1267(1476)
MDU	1128(215)	1033(197)	525	1921(366)	13857(2637)
PC	231(185)	228(182)	125	494(395)	2017(1612)
PBC	36(227)	34(214)	16	67(424)	433(2744)
PMU	812(221)	721(196)	368	1235(336)	10461(2844)
PVA	306(210)	303(208)	146	526(361)	2624(1801)
PVM	3250(220)	2884(195)	1475	4941(335)	38757(2627)
SCD	121(189)	121(188)	64	277(432)	983(1532)

4.2.2 Area

Table 13 shows the area of the units in an RSD core. Although there is no difference between cell area of CNFET5 and CNFET7, the table shows that the area of CNFET5 is slightly larger than that of CNFET7. This is similar to the result shown in our previous work [24], which shows the area of the units in an OpenSPARC T2 core after logic synthesis. The table also shows that the area of CNFET7 is almost 2x

Table 14: Delay of RSD. The units of the numbers without parentheses are *ps*. The numbers within parentheses represent percentages against ASAP7.

Unit	CNFET5	CNFET7	ASAP7	Path
CSRU	493.6(60.2)	685.8(83.6)	820.6	reg2reg
IOU	735.1(102.8)	811.6(113.4)	715.2	default
LSU	175.4(137.1)	173.4(135.5)	106.1	reg2reg
MDU	679.5(67.2)	673.6(66.7)	1010.5	default
PC	290.1(130.3)	309.6(139.1)	222.6	reg2reg
PBC	28.6(73.5)	32.1(82.4)	38.9	reg2reg
PMU	180.5(25.8)	119.8(17.1)	698.8	default
PVA	644.7(81.9)	771.1(97.9)	787.6	default
PVM	493.4(58.6)	304.6(36.2)	841.5	default
SCD	70.1(114.0)	69.0(112.3)	61.4	regreg

larger than that of ASAP7.

4.2.3 Delay

When we measure unit delay, we focus on a path from a register to a register (reg2reg) for CSRU, LSU, PC, PBC and SCD because these units are related to registers tightly. With respect to the rest of the units, the default paths are used for our experiment.

Table 14 shows the delay of the units in an RSD core. As can be seen from the table, CNFET5 and CNFET7 show smaller delay ASAP7 for many units. However, a few units such as IOU show large delay for CNFET5 and CNFET7 when compared to ASAP7. This may be influenced by the inaccuracy of our delay prediction method, as well as the experimental results shown in Section 4.1.3. Our future work is to improve the accuracy of our delay prediction method.

5. Related Work

In addition to the in-depth study of CNFET by Hill et al. mentioned above[6][5][7], some other related studies are equally informative for this paper.

A.K. Kureshi et al. compared the performance of CNFET and CMOS in 32nm node based on 6T SRAM[9] in 2009. In the final conclusions, CNFET-based 6T SRAM cell provides an improvement of 21% in read static noise margin (SNM) and 1.84 × faster than CMOS cell. The standby leakage of CNFET cell is 84% less than CMOS cell. This provides us with experimental ideas and methods for future work on megacells.

Geunho Cho et al. evaluated the performance of CNFET-based logic gates in 32nm node in 2009[2]. The results show that the power-delay product (PDP) and the leakage power for the CNFET based gates are lower than the MOSFET based logic gates by 100 to 150 times, respectively. Having reference results from the gate level is a very helpful guide in the experimental process.

6. Conclusions

In this paper, we showed the power consumption, area, and delay of various units in OpenSPARC T2 and RSD cores after place and route. With respect to OpenSPARC T2, CNFET7 can reduce total power consumption by up to 94.6% (PKU) and leakage power by up to 64.6% (DEC) at expense of 1.7x area overhead when compared to ASAP7, while CNFET5 can reduce total power consumption by up to 38% (DEC) and leakage power by up to 41% (IFU_IBU) with the same area overhead when compared to CNFET7 With respect to RSD, CNFET7 can reduce total power consumption (PVA) by up to 94.5%, leakage power by 65.4% (LSU) and delay by up to 82.9% at expense of 2x area overehad when compared to ASAP7, while CNFET5 can reduce total power consumption by up to 32% (PVM) and leakage power by up to 46.5% (PVM) with the same area overhead when compared to CNFET7.

In the future, in order to improve the accuracy of the whole experiment, we will use Virtuoso to generate LEF files based on some early studies, which can more accurately describe the physical information of CNFET. Also, we will try to use Synopsys' IC Compiler to do the same experiment and compare the results with Innovus to get a more solid conclusions.

In this paper, we did not place and route all units within the processors due to the lack of SRAM macros in our CNFET PDKs and therefore will try to generate SRAM macros for the PDKs. After that, we will perform place and route for all units in the processors and then show the power consumption, area, and delay of each unit.

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References

[1] Arizona State University: ASAP: Arizona State Predictive PDK, *Internet:asap.asu.edu/asap/* ([February 1, 2022]).
[2] Cho, G., Kim, Y.-B., Lombardi, F. and Choi, M.: Performance evaluation of CNFET-based logic gates, *2009 IEEE Instrumentation and Measurement Technology Conference*, pp. 909–912 (online), DOI: 10.1109/IMTC.2009.5168580 (2009).
[3] Clark, L. T., Vashishtha, V., Shifren, L., Gujja, A., Sinha, S., Cline, B., Ramamurthy, C. and Yeric, G.: ASAP7: A 7-nm finFET predictive process design kit, *Microelectronics Journal*, Vol. 53, pp. 105–115 (online), DOI: https://doi.org/10.1016/j.mejo.2016.04.006 (2016).
[4] Eeckhout, L.: Is Moore's Law Slowing Down? What's Next?, *IEEE Micro*, Vol. 37, No. 04, pp. 4–5 (2017).
[5] Hill, G.: Variation-aware Nanosystem Design Kit (NDK), *Internet:nanohub.org/resources/22582* (July 29, 2015 [June 9, 2021]).
[6] Hills, G., Bardon, M. G., Doornbos, G., Yakimets, D., Schuddinck, P., Baert, R., Jang, D., Mattii, L., Sherazi, S. M. Y., Rodopoulos, D., Ritzenthaler, R., Lee, C.-S., Thean, A. V.-Y., Radu, I., Spessot, A., Debacker, P., Catthoor, F., Raghavan, P., Shulaker, M. M., Wong, H.-S. P. and Mitra, S.: Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI, *IEEE Transactions on Nanotechnology*, Vol. 17, pp. 1259–1269 (2018).
[7] Hills, G., Lau, C., Wright, A., Fuller, S., Bishop, M. D., Srimani, T., Kanhaiya, P., Ho, R., Amer, A., Stein, Y., Murphy, D., Arvind, Chandrakasan, A. and Shulaker, M. M.: Modern Microprocessor Built from Complementary Carbon Nanotube Transistors, *Nature*, Vol. 572, pp. 595—602 (2019).
[8] IRDS: International Roadmap for Devices and Systems 2018 –Beyond CMOS–, Whitepaper (2018).
[9] Kureshi, A. and Hasan, M.: Performance comparison of CNFET- and CMOS-based 6T SRAM cell in deep submicron, *Microelectronics Journal*, Vol. 40, No. 6, pp.

979–982 (online), DOI: https://doi.org/10.1016/j.mejo.2008.11.062 (2009).

[10] Luisier, M. and Klimeck, G.: Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors, *IEEE Electron Device Letters*, Vol. 30, No. 6, pp. 602–604 (2009).

[11] Martins, M. G. A., Matos, J. M., Ribas, R. P., Reis, A. I., Schlinker, G., Rech, L. and Michelsen, J.: Open Cell Library in 15nm FreePDK Technology, *Proceedings of the 2015 Symposium on International Symposium on Physical Design* (2015).

[12] Mashimo, S., Fujita, A., Matsuo, R., Akaki, S., Fukuda, A., Koizumi, T., Kadomoto, J., Irie, H., Goshima, M., Inoue, K. and Shioya, R.: An Open Source FPGA-Optimized Out-of-Order RISC-V Soft Processor, *2019 International Conference on Field-Programmable Technology (ICFPT)*, pp. 63–71 (online), DOI: 10.1109/ICFPT47387.2019.00016 (2019).

[13] NC State University: FreePDK, *Internet:www.eda.ncsu.edu/wiki/FreePDK* (May 29, 2014 [June 10, 2021]).

[14] Nishizawa, S., Lin, S.-T., Li, Y.-L. and Onodera, H.: Supplemental PDK for ASAP7 Using Synopsys Flow, *IPSJ Transactions on System LSI Design Methodology*, Vol. 14, pp. 24–26 (online), DOI: 10.2197/ipsjtsldm.14.24 (2021).

[15] Qiu, C., Zhang, Z., Xiao, M., Yang, Y., Zhong, D. and Peng, L.-M.: Scaling Carbon Nanotube Complementary Transistors to 5-nm Gate Lengths, *Science*, Vol. 355, pp. 271–276 (2017).

[16] Saini, P. and Mehra, R.: Leakage power reduction in CMOS VLSI circuits, *International Journal of Computer Applications*, Vol. 55, No. 8 (2012).

[17] Sasaki, T., Ando, Y., Kameno, M., Tahara, T., Koike, H., Oikawa, T., Suzuki, T. and Shiraishi, M.: Spin Transport in Nondegenerate Si with a Spin MOSFET Structure at Room Temperature, *Physical Review Applied*, Vol. 2, p. 034005 (2014).

[18] Shioya, R. et al.: RSD RISC-V Out-of-Order Superscalar Processor, *Internet:github.com/rsd-devel/rsd* ([February 2, 2022]).

[19] Silicon Integration Initiative: 15nm Open-Cell Library and 45nm FreePDK, *Internet:si2.org/open-cell-library/* ([June 10, 2021]).

[20] Simonite, T.: IBM: Commercial Nanotube Transistors Are Coming Soon, *Internet:www.technologyreview.com/2014/07/01/172177/ibm-commercial-nanotube-transistors-are-coming-soon/* (July 1, 2014 [June 9, 2021]).

[21] Stanford Nanoelectronics Lab: VS-CNFET Model, *Internet:nano.stanford.edu/stanford-cnfet2-model* (July 2, 2021 [June 10, 2021]).

[22] Sun Microsystems: OpenSPARC T2 Core Microarchitecture Specification, Whitepaper (2007).

[23] Sun Microsystems: OpenSPARC T2 Processor Megacell Specification, Whitepaper (2007).

[24] 佐々木魁，三輪　忍，ヨウドウキン，塩谷亮太，八巻隼人，本多弘樹カーボンナノチューブトランジスタを用いて論理合成したプロセッサの電力/面積/回路遅延評価，技術報告 4 (2021).