Applying Feature Models to the Dynamic Partial Reconfiguration Process

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Abstract: FPGAs (Field Programmable Gate Arrays) are widely used in various accelerator development such as image processing and deep learning. Dynamic Partial Reconfiguration (DPR) is a useful technique on FPGAs. DRP can change the FPGA functionality by loading partial bit-streams without stopping circuit. FPGA design flow using DPR has following steps: (1) synthesize each module, (2) define reconfigurable partition setting, (3) save routing data between static module and a reconfigurable module as design checkpoint, (4) repeat step (3) to the number of reconfigurable modules, (5) generate bit-stream for each configuration. In particular, FPGA designers have to repeat the placement and routing work in step (3) to add a reconfigurable module. Therefore, the design complexity increases in proportion to the number of reconfigurable modules. In this research, we propose the applying feature models to the DPR-design process to support simple description to realize management of FPGA system using DPR. Feature model can represent variability utilizing a tree structure. In our approach, we generate information of placement and routing from a feature model, and required features are synthesized as static modules. On the other hand, optional features and alternative features are synthesized as reconfigurable modules. This DPR design process using Feature Model is effective to manage module structure. In the future, we design this approach minutely, realize our method, and simplify design process of FPGA system using DPR.

Keywords: FPGA, Dynamic Partial Reconfiguration, Feature Model

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