C-008

A High Density Escape Routing Method for Staggered-Pin-Array Based Mixed-Pattern Signal Model

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Abstract　Escape routing is one of key problems in design of printed circuit boards (PCB), and it becomes more and more difficult for manual design due to increased pin count. This paper proposed an algorithm using an unified model to formulate the problem of escape routing of differential pairs together with single signals (mixed-pattern signals) on staggered pin array(SPA) considering the routing's density.

Keywords　PCB Escape Routing, Mixed-Pattern Signals, Staggered-Pin-Array, Linear Programming

1. Introduction

Escape routing is aimed at routing nets from pins to the boundary of the components on PCB. The escape routing can be divided into two classes: single signals escape routing and differential pair escape routing. For the single signal routing, there is only one net for each signal. While, differential pair escape routing requires completely parallel dual nets for some pin pairs.

Ref.[1] proposed an algorithm to solve escape routing which takes both differential-pair and single signals into consideration, but it loses sight of high density. Ref.[2] proposed an algorithm to solve escape routing which use orthogonal-side wiring style that fully utilizes the routing resource to ensure the high density, but it only contains the single signals.

In this paper, we propose an algorithm which takes both differential pairs signals routing and high routing density into consideration.

2. Preliminaries

2.1 Routing Network

Fig.1 shows a triangular-tile model [2] of routing network which triangular region in the staggered pin array formed by three adjacent pins. In this routing network, we create two extra nodes: source node and sink node. Source node is connected to all escape pins, while sink node is connected to all boundary nodes.
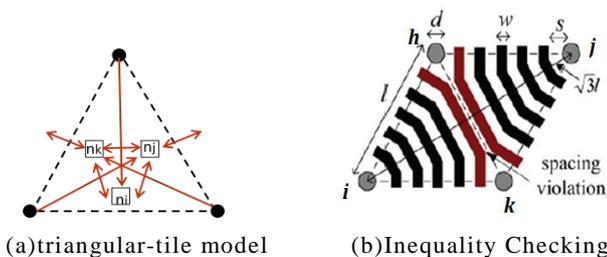

(a)triangular-tile model　　　(b)Inequality Checking

Figure 1 Routing network model

2.2 Formulation

The high density escape routing method for staggered-pin-array based mixed-pattern signal model can be defined as follows:

Input: a) size of staggered pin array,

b) the number and coordinates of the differential-pairs signals and single signals

c) the DRC rules including wire width, wire spacing, pin diameter

Output: the routing of each signal

Constraints: a) two nets of one differential-pair signal should be routed from pins to boundary at the same time,

b) routings can't intersect with each other,

Object: a) $min \sum_{e_{i,j}} l(e_{i,j}) f(e_{i,j})$

b) the nets which are routed from pins to boundary is as many as possible.

3. Proposed Algorithm

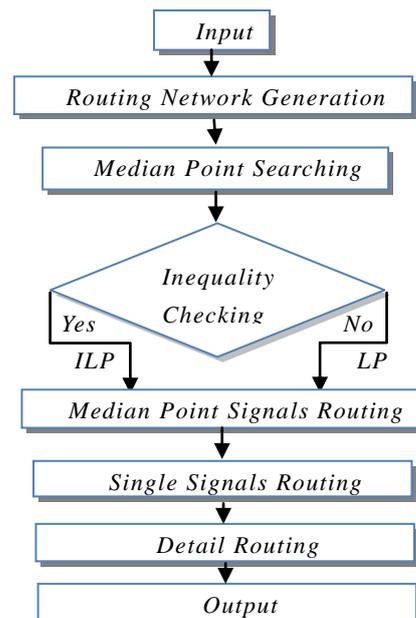Fig.2 shows an overview of the proposed algorithm.

Figure 2: Overview of the algorithm

3.1 Routing Network Generation

The model of the routing network is shown in the Fig1. Given P_D: the set of escaped differential-pair pins, P_S: the set of escaped single pins, P_U: the set of nonescaped pins, and N: the set of internal nodes and boundary nodes, the routing network is G=(V,E), where V=P∪N and $P=P_D$ ∪P_S ∪P_U.

3.2 Median Points Searching

We use the breath-first-search(BFS) to search the median points of differential-pairs[1].

3.3 Inequality Checking

When we use the orthogonal-side wiring routing style, here comes the following question as shown in Fig.1(b).

$$\left|\frac{2 \times (l-d) - 2 \times s}{w+s}\right| > \left|\frac{\sqrt{3l}-d-s}{w+s}\right| \qquad (1)$$

If the inequality does not hold, use the LP formulation. Otherwise, use ILP formulation.[2]

3.4 LP Formulation

1) $l(e_{i,j})$ denotes the length of edge $e_{i,j}$;

2) $f(e_{i,j})$ denotes the flow of edge $e_{i,j}$.

3) $c(e_{i,j})$ denotes the capacity of edge $e_{i,j}$. If $i \in P$, $c(e_{i,j}) = 1$. If $i,j \in N$, and i,j are not in the same tile, $c(e_{i,j}) =$ **maximum of wires**. For other edge, the $c(e_{i,j})$ is infinite.

3.4.1 Median-point signals routing

The LP formulation is as follows: $min \sum_{e_{i,j}} l(e_{i,j}) f(e_{i,j})$

Subject to: $\qquad \sum_{e_{i,j} \in E} f(e_{i,j}) = 2, \forall i \in P_D,$ $\quad$ **(2)**

$\sum_{e_{i,j} \in E} f(e_{i,j}) = 2 * |P_D|, \forall i \text{ is the source},$ $\quad$ **(3)**

$\sum_{e_{i,j} \in E} f(e_{i,j}) = 2 * |P_D|, \forall j \text{ is the sink},$ $\quad$ **(4)**

$\sum_{e_{i,j} \in E} f(e_{i,j}) = \sum_{e_{j,k} \in E} f(e_{j,k}), \forall j \in P \cup N,$ $\quad$ **(5)**

$f(e_{i,j}) \le c(e_{i,j}), \forall e_{i,j} \in E,$ $\quad$ **(6)** $\quad \forall f(e_{i,j}) \ge 0.$ $\quad$ **(7)**

Constraint (2) ensures that there is no reiteration in each escape pin node. Constraint (3) and (4) ensure that every escape pin will be routed from the source node to the sink node. Constraint (5) ensures the total flow income of a node equals the total output flow from the node. And constraint (6) ensures the flow of an edge cannot exceed its capacity. Constraint (7) makes the flow on all edges nonnegative.

3.4.2 Single Signals Routing

The LP formulation as follows: $min \sum_{e_{i,j}} l(e_{i,j}) f(e_{i,j})$

Subject to: $\qquad \sum_{e_{i,j} \in E} f(e_{i,j}) = 1, \forall i \in P_S,$ $\quad$ **(8)**

$\sum_{e_{i,j} \in E} f(e_{i,j}) = |P_S|, \forall i \text{ is the source},$ $\quad$ **(9)**

$\sum_{e_{i,j} \in E} f(e_{i,j}) = |P_S|, \forall j \text{ is the sink},$ $\quad$ **(10)**

$\sum_{e_{i,j} \in E} f(e_{i,j}) = \sum_{e_{j,k} \in E} f(e_{j,k}), \forall j \in P \cup N,$ $\quad$ **(11)**

$c(e_{i,j}) = \begin{cases} c(e_{i,j}) - 2, \forall e_{i,j} \in E_D \\ c(e_{i,j}), e_{i,j} \text{ not belong to } E_D \end{cases},$ $\quad$ **(12)**

$f(e_{i,j}) \le c(e_{i,j}), \forall e_{i,j} \in E,$ $\quad$ **(13)** $\quad \forall f(e_{i,j}) \ge 0.$ $\quad$ **(14)**

Constraints (8) to (11) just like the constraints (2) to (5).

Constraint (12) takes the edges that used in the routings of differential-pair signals into consideration. And constraint (13) ensures the flow of an edge cannot exceed its capacity. Constraint (14) makes the flow on all edges nonnegative.

3.5 ILP Formulation

Under this circumstance, we have to consider two triangular tiles together to figure this problem. Like Fig.4 is the model that consider the wires between p_j and p_h. $\varphi(p_j, p_h)$ is defined as the maximum routing number between pins p_j and p_h. U_{p_j,p_h} is defined as the set of edges showed in the Fig.3.
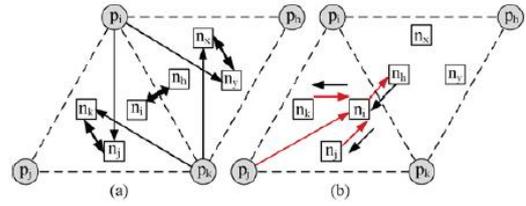

Figure 3: Extra constraints for avoiding spacing violation

The added constraints are as follow:

$$\sum_{e_{i,k} \in U_{p_i,p_h}} f(e_{i,j}) \le \varphi(p_i, p_h), \qquad (15)$$

$$f(e_{n_k,n_i}) + f(e_{n_j,n_i}) + f(e_{p_j,n_i}) = f(e_{n_i,n_h}), \qquad (16)$$

$$f(e_{n_h,n_i}) = f(e_{n_i,n_k}) + f(e_{n_i,n_j}), \qquad (17)$$

$$\forall f(e_{i,j}) \in Z_0^+. \qquad (18)$$

With the constraint (2) to (7) and (15) to (18), we can get the integer number of the flows on each edge in the ILP formulation when solving the median point signals routing. Then with the constraint (8) to (18), we can get the integer number of the flows on each edge when solving the single signals routing. Thus, the detailed routing can be performed successfully.

4. Conclusion

The proposed algorithm ensures the mixed-pattern signals can be routed from pins to boundary with a high routing density. Besides, the total length of routings is as short as possible by using LP/ILP.

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