RC-010

# A Method for Aging Estimation of CMOS Circuits Using Ring Oscillators

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Abstract

*NBTI, PBTI, and CHC aging occurs in nanoscale transistors and is one of the factors that degrades the performance of LSIs. Aging decreases the operating speed of a transistor, causing the LSI to ultimately malfunction due to increment in the signal propagation delay time. This paper presents a method for estimating the amount of increment in the delay time of an LSI and a method for estimating the amount of increment in the threshold voltage per transistor from the changes in the period of two ring oscillators by aging. Results of circuit simulations showed that the proposed methods can perform estimations with an error rate of less than 4.6 % for the delay time increment and less than 0.6 % for the threshold voltage increment.*

***Keywords****: Aging (Degradation), Delay time, MOS FET, Ring oscillators, NBTI, PBTI, CHC*

## 1. Introduction

The negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), and channel hot carrier (CHC) aging (degradation) of MOS FETs is one of the factors that reduces the performance of an LSI as the size of CMOS devices continues to shrink [1]-[3]. When a negative (positive) bias voltage is applied to the gate terminal of a PMOS FET (NMOS FET), NBTI (PBTI) aging occurs and the threshold voltage of the PMOS FET (NMOS FET), $|V_{thp}|$ ($|V_{thn}|$) (absolute value), increases. CHC aging also occurs when the NMOS FET turns on, resulting in an increase to the threshold voltage of the NMOS FET, $|V_{thn}|$ (absolute value).

If the threshold voltage $|V_{th}|$ of the MOS FET increases due to aging, the switching speed of the MOS FET decreases and the delay time of the path in the LSI chip also increases. As the increased delay time is very small (e.g., on the ps order for deep submicron technology), it is difficult to accurately measure the delay time from outside of the chip. To estimate LSI aging, it is therefore necessary to measure the propagation delay time of the path by using a measurement circuit built in to the LSI chip [4]. For this purpose, several built-in methods to measure the delay time caused by aging have been proposed [4-9].

In the methods proposed by [5]-[8], a critical path (i.e., a path of the largest propagation delay time) in the LSI is first selected at the design stage. A circuit to measure the propagation delay time of the critical path is embedded in the LSI and it judges whether or not the measured propagation delay time is within a design margin. When the delay time becomes large, resulting in the time margin becoming small, a warning signal is output. However, such methods can only measure the delay time of one pre-selected path. The method of [4] selects not only the critical path but also semi-critical paths at the design stage, and an embedded circuit can measure the propagation delay times of these multiple paths. However, the size of the measuring circuit increases as the number of measured paths grows. The method of [9] features ring oscillators (ROs) embedded in the LSI chip that are used to measure the propagation delay time influenced by MOS FET aging. This method uses two different ROs: one affected by PBTI, NBTI, and CHC and the other affected by PBTI and NBTI. Although this method can estimate the influence of aging for each kind of aging, it only estimates the amount of aging of MOS FETs used in ROs.

The above methods require the circuit for measuring the propagation delay time of a specific path(s) to be embedded at the LSI design stage. They cannot measure the propagation delay times of arbitrary paths increased by aging after LSI manufacturing. Under the long-term use of an LSI chip, the critical path frequently changes to another path because the increment ratio of the propagation delay time by aging is different for every path [10]. Therefore, it is necessary to measure the propagation delay times of multiple paths. In addition, the above methods cannot estimate the amount of aging at the MOS FET level. In this paper, we propose a method for estimating the delay time of the MOS FET, $\Delta tsd$ (increased switching delay), and the threshold voltage of the MOS FET, $\Delta V_{th}$ (increased threshold voltage), both of which are increased by aging. We also propose a method for estimating the propagation delay time increased by aging, $\Delta tpd$ (increased path delay), of any path in the LSI chip.

This paper is organized as follows. Section 2 outlines our proposed method for estimating a MOS FET aging and Section 3 describes circuit structures of ROs and their behaviors used for the aging estimation method. In Section 4, we describe the aging estimation method. Section 5 presents our evaluation and considerations of the estimation method by means of circuit simulations. We conclude with a brief summary in Section 6.

## 2. Aging estimation procedure

To estimate the aging of an LSI chip, the proposed method uses two kinds of ring oscillators (ROs) embedded in the LSI chip and utilizes their oscillation periods. First, we give an overview of the ROs. The RO is an oscillator consisting of odd numbered inversion-type gates that are connected like a ring. Its oscillation period corresponds to

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the summation of the propagation delay times of all gates configuring the RO. The propagation delay time of a gate is determined by the delay time of the switching (i.e., switching time) behavior of the MOS FET. Thus, the oscillation period can be calculated from the switching time of the MOS FET. The switching time is calculated from an RC circuit model consisting of an on-resistance $R_{on}$ and a load capacitance $C$ of the MOS FET. An RC circuit model is used because it enables a simplified calculation model and the delay time can be calculated with relatively high accuracy. The switching delay time, *tsd*, per MOS FET is expressed as [11]

$$tsd = 0.69 \cdot R_{on} \cdot C \,. \quad (1)$$

The initial oscillation period, $T_{init}$, of the RO is expressed by

$$T_{init} = 2 \cdot n \cdot k \cdot tsd \,, \quad (2)$$

where $n$ is the number of gates and $k$ is a coefficient determined by a circuit structure such as a parallel connection or a serial connection of MOS FETs in the gate [11].

When both of the PMOS FET and NMOS FET experience aging, the threshold voltage $|V_{th}|$ of the MOS FET increases and then the on-resistance increases by $\Delta R_{on}$ [11]. When the on-resistance of the MOS FET increases by $\Delta R_{on}$ and the switching time per MOS FET increases by $\Delta tsd$, the oscillation period of the RO from (1) and (2) is expressed as

$$T = T_{init} + 2 \cdot n \cdot k \cdot \Delta tsd \,. \quad (3)$$

Two different kinds of ROs consist of gates provided by a standard cell library. Oscillation and non-oscillation modes of ROs can be switched by applying a control signal. Except for the measurement interval of the oscillation periods of ROs, the two ROs are always in the non-oscillation mode. In this setup, one RO is designed so that the PMOS FET does not receive the effect of the NBTI aging and the NMOS FET instead causes its own aging (NMOS-aged RO (i.e., PMOS-aging tolerant RO)) while the other is designed so that the NMOS FET does not receive the effect of the PBTI and CHC aging and the PMOS FET instead causes its own aging (PMOS-aged RO (i.e., NMOS-aging tolerant RO)) [13]. Therefore, as their aging is influenced only by either a PMOS FET or NMOS FET, $n$ MOS FETs receive their own aging during one oscillation period and the propagation delay time of the RO increases Thus, the oscillation period of the NMOS-aged RO, $T_n$, is expressed by

$$T_n = T_{n\_init} + n \cdot k \cdot \Delta tsdn \,, \quad (4)$$

where $\Delta tsdn$ is the delay time of one NMOS FET increased by its aging. The oscillation period of the PMOS-aged RO, $T_p$, is obtained in the same manner.

Next, we present the outline of the aging estimation method using the two ROs (Fig. 1). From (4), the increased delay time of one NMOS FET, $\Delta tsdn$, is expressed by

$$\Delta tsdn = \frac{T_n - T_{n\_init}}{n \cdot k} \,. \quad (5)$$

The increased delay time of one PMOS FET, $\Delta tsdp$, is obtained in the same manner. Therefore, $\Delta tsdn$ and $\Delta tsdp$ can be calculated from $T_n$ and $T_p$, which are the measurement values of the oscillation periods for the two ROs embedded in the LSI chip, and $T_{n\_init}$ and $T_{p\_init}$, which are the initial oscillation periods for the two ROs at the time of factory shipment (i.e., values without aging).

In the proposed method, the $T_n$ and $T_p$ oscillation periods of the two ROs embedded in the LSI chip are measured first (Fig. 1, S1). When the initial oscillation periods of these ROs (i.e. oscillation periods without aging), $T_{n\_init}$ and $T_{p\_init}$, are known, these periods are used for calculation. If the initial periods are unknown, they are calculated from a calculation model described in Section 3 and from the MOS FET parameters (Fig. 1, S2). Increased delay times, $\Delta tsdn$ and $\Delta tsdp$, are calculated from (5) by using those measured periods of ROs and initial periods (Fig. 1, S3).

The amount of the threshold voltage of the MOS FET increased by aging, $\Delta V_{th}$, is estimated second. Converting the equation of the calculation model for $\Delta tsd$, which has the variable for the threshold of the MOS FET, generates the function of $V_{th}=f(\Delta tsd)$ (Fig. 1, S4). When $\Delta tsdn$ and $\Delta tsdp$ are applied to the function, the threshold voltage $|V_{th}|$ of the MOS FET in the LSI chip is obtained. Calculating the difference between those calculated values and initial threshold voltages (i.e., values without aging), the threshold voltage of the MOS FET increased by aging, $\Delta V_{th}$, is estimated (Fig. 1, S5).

Third, the obtained $\Delta tsdn$ and $\Delta tsdp$ are changed into the propagation delay time of the gate, $\Delta tdg$, in the LSI chip increased by aging (Fig. 1, S6). A calculation model for all kinds of gates has been provided in advance. As the delay time of one gate depends on its own input value, the maximum delay time is assumed at the time of calculation. The number of fan-outs and the rising/falling time of the input signal are also considered for calculating the delay time. Applying the increased delay time of each gate obtained from the above to an arbitrary path in the LSI chip, the maximum delay time of the path, $\Delta tpd$, increased by aging is estimated (Fig. 1, S7).

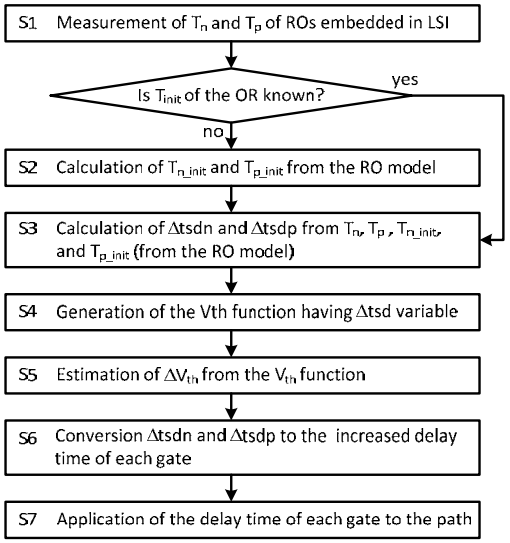
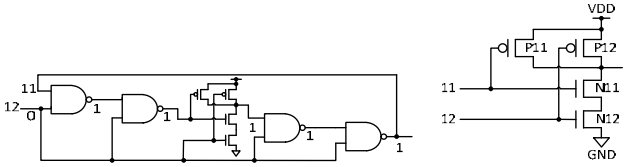



Figure 1 Outline of the aging estimation method.

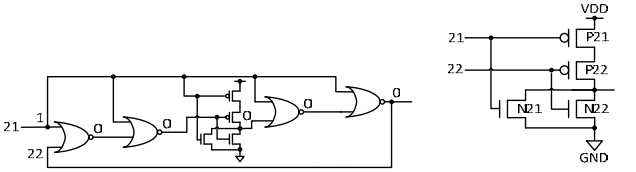
## 3. RO structures and their behaviors

Figs. 2 and 3 show two ROs [13]. In this paper, we explain the NMOS-aged RO (i.e., PMOS-aging tolerant RO). Fig. 2(a) shows the gate level diagram and Fig. 2(b) shows its MOS FET level diagram. The OR enters the oscillation mode when logic 1 is applied to control signal line 12 and enters the non-oscillation mode when logic 0 is applied to the control signal line. Fig. 2(a) also shows the logic values in the RO for the non-oscillation mode. MOS FETs used for oscillation are P11, N11, and N12 (see Fig. 2(b)). In the non-oscillation mode, P12 and N11 are on-state and P11 is off-state (i.e., P11 is not affected by the NBTI aging). By using the OR, therefore, it is possible to measure the oscillation period that is not influenced by the NBTI aging of P11. However, the aging of N11 such as PBTI and CHC progresses. Similarly, when the RO consisting of NOR gates is used, a PMOS-aged RO (i.e., NMOS-aging tolerant RO) is realized (Figs. 3(a) and (b)).




(a) non-oscillation mode (b) MOS FET level

Figure 2 NMOS-aged RO.




(a) non-oscillation mode (b) MOS FET level

Figure 3 PMOS-aged RO.

## 4. Aging estimation method

In this section, we first explain the calculation model used for the aging estimation in detail. The oscillation periods of two kinds of ROs can be modeled by the RC circuit consisting of the $R_{on}$ and $C$ of the MOS FET. In the following, we discuss the model of the NMOS-aged RO as an example.

The on-resistance $R_{on}$ is calculated by [11]:

$$R_{on} = \frac{V_{ds}}{I_{ds}}\,, \tag{6}$$

where $V_{ds}$ is the drain-source voltage and $I_{ds}$ is the drain-source current of the MOS FET.

$I_{ds}$ is given by the alpha-power low MOS FET model [12]:

$$I_{ds} = \frac{1}{2}\cdot\mu_{eff}\cdot\frac{\varepsilon_{ox}}{t_{ox}}\cdot\frac{W}{L}\cdot\left(V_{gs}-V_{th}\right)^{\alpha}\cdot(1+\lambda\cdot V_{ds})\,, \tag{7}$$

where $\mu_{eff}$ is the effective mobility, $\varepsilon_{ox}$ is the dielectric constant of the gate oxide, $t_{ox}$ is the gate oxide thickness, $W$ and $L$ are the channel width and length, respectively, $V_{gs}$ is the gate-source voltage, $V_{th}$ is the threshold voltage, and $\lambda$ is the channel length modulation parameter.

$V_{th}$ is calculated considering a substrate bias effect [14]:

$$V_{th} = V_{th0} + K1\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right) - K2\cdot V_{bs}\,. \tag{8}$$

where $V_{th0}$ is the zero-bias threshold voltage. $K1$ and $K2$ are the body bias coefficient, $\Phi_s$ is the surface potential, and $V_{bs}$ is the bulk-source voltage.

The capacitance of the MOS FET, $C$, consists of a gate oxide capacitance $C_{ox}$, a junction capacitance $C_{js}$/$C_{jd}$, and an overlap capacitance $C_{gs}$/$C_{gd}$ (i.e., $C$=$C_{ox}$+$C_{js}$+$C_{jd}$+$C_{gs}$+$C_{gd}$) whose values are respectively calculated by (9), (10), and (11) (Fig. 4) [11]:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}\cdot L\cdot W\,, \tag{9}$$

$$C_{js,d} = \frac{cj\cdot A_{s,d}}{\left(1+\frac{V_{s,db}}{pb}\right)^{mj}} + \frac{cjsw\cdot P_{s,d}}{\left(1+\frac{V_{s,db}}{pbsw}\right)^{mjsw}}\,, \tag{10}$$

$$C_{gs} = C_{gd} = CGSO\cdot W = CGDO\cdot W\,, \tag{11}$$

where *cj* and *cjsw* are the zero-bias depletion capacitances of the bottom and sidewalls, respectively, $A_{s,d}$ and $P_{s,d}$ are the area and perimeter of the source of drain implant, respectively, $V_{s,db}$ is the potential from the source or drain to the body, *pb* and *pbsw* are the built-in potential for the bottom and sidewall components, respectively, *mj* and *mjsw* are the grading coefficients for the bottom and sidewall components, respectively, and finally *CGSO* and *CGDO* are the gate-source and gate-drain overlap capacitances, respectively.

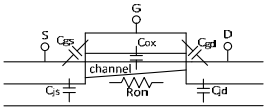
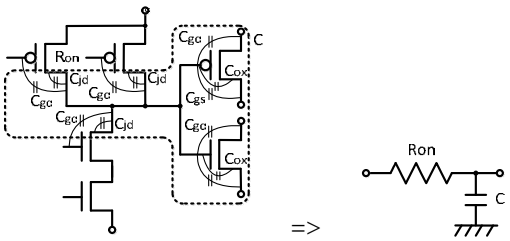
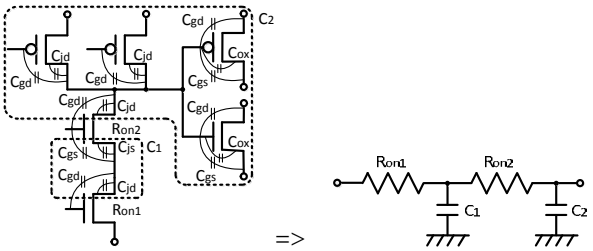



Figure 4 Capacitance model of the MOS FET.




(a) *tpLH*(n) and *tpHL*(p)




(b) *tpHL*(n) and *tpLH*(p)

Figure 5 RC circuit model.

The oscillation period of the RO is obtained from the summation of the propagation delay time of each gate in the RO. Here, the propagation delay time is given by *tpLH*

and *tpHL*, which are the differences between input and output voltages when they reach up to 50% of the VDD.

Suppose the propagation delay times per gate in the NMOS-aged RO (PMOS-aged RO) are *tpLH*(n) and *tpHL*(n) (*tpLH*(p) and *tpHL*(p)). When the propagation delay times of *tpLH*(n) and *tpHL*(p) occur, only one MOS FET among two parallel-connected MOS FETs is in an on-state in the gate. Then, $k$=1 in (2) and its circuit model is as shown in Fig. 5(a). When the propagation delay times of *tpHL*(n) and *tpLH*(p) occur, both MOS FETs comprising the two serial-connected MOS FETs are in an on-state in the gate. Then, $k$=2 in (2) and its circuit model is as shown in Fig. 5(b). Therefore, the calculation model of the propagation delay time per gate of the NMOS-aged RO is expressed by [11]:

$$tpLH(n) = 0.69 \cdot R_{onp} \cdot \left(2C_{jdp} + 2C_{jdp} + C_{jdn} + C_{gdn} + C_{gdn} + C_{gsn} + C_{oxn} + C_{gdp} + C_{gsp} + C_{oxp}\right), \quad (12)$$

$$tpHL(n) = 0.69 \cdot 2R_{onn} \cdot \left\{\left(2C_{jdp} + 2C_{jdp} + C_{jdn} + C_{gdn} + C_{gdn} + C_{gsn} + C_{oxn} + C_{gdp} + C_{gsp} + C_{oxp}\right) + \frac{1}{2} \cdot \left(C_{jdn} + C_{gdn} + C_{jsn} + C_{gsn}\right)\right\}, \quad (13)$$

where symbols with the suffix $p$ and $n$ represent parameters for PMOS FET and NMOS FET, respectively.

As the summation of *tpLH* and *tpHL* is the propagation delay time per gate for one oscillation period, the calculation model for the oscillation period, $T_n$, of the NMOS-aged RO is expressed by

$$Tn = (tpLH(n) + tpHL(n)) \cdot n \cdot a\,, \quad (14)$$

where $a$ is a fitting coefficient for correcting the value of the oscillation period [15].

Supposing $T_n$ is the oscillation period of the NMOS-aged RO embedded in the LSI chip (i.e., measured value), from (5), the calculation model of the increased delay time of one NMOS FET, Δ*tsdn*, is expressed by (15). If the initial oscillation period, $T_{n\_int}$, of the NMOS-aged RO is known, its value is used for (15). However, if it is unknown, it can be calculated from (2).

$$\Delta tsdn = \frac{T_n - T_{n\_init}}{2n} \quad (15)$$

Now, we explain the calculation method of $\Delta V_{th}$ (the threshold voltage increased by aging). Suppose Δ*tsdn* and Δ*tsdp* are obtained from (15) and $T_{n\_init}$ and $T_{p\_init}$ are obtained from (2). In this case, the equations of Δ*tsd* (Δ*tsdn* and Δ*tsdp*) can be expressed by the function with the variable of $V_{th}$ as

$$\Delta tsd = f(V_{th})\,. \quad (16)$$

Converting (16), we obtain

$$g(\Delta tsd, V_{th}) = 0\,. \quad (17)$$

As Δ*tsd* is a known value, (17) is a high-degree equation with the variable of $V_{th}$. By solving (17), the $V_{th}$ increase by aging is obtained. MATLAB is used for solving Eq. (17). Therefore, $\Delta V_{th}$ is calculated by the difference between the estimated $V_{th}$ from (17) and the initial $V_{th}$ (i.e., without aging).

Next, we explain the estimation method of the maximum delay time of a path. The increased delay time of one NMOS FET, Δ*tsdn*, obtained from (15) is first converted to the increased delay time of each gate used in the LSI chip. Suppose Δ*tsd* is estimated by (15) and $\Delta V_{th}$ is estimated by (17). In addition, the increased delay time of each gate, Δ*tdg*, is calculated as the increased *tpHL* and *tpLH* by using the RC circuit considering the gate structure and the above Δ*tsd* and $\Delta V_{th}$. Then, a conversion coefficient $w$ that converts Δ*tsd* (i.e., Δ*tsdn* and Δ*tsdp*) into the maximum increased delay time of the gate, Δ*tdg*, is calculated as

$$w = \frac{\Delta tdg}{\Delta tsd}\,. \quad (18)$$

The gate delay time depends on both the transition time of the input signal (i.e., rising time and falling time) and the number of fan-outs (i.e., load capacitance) [11], [12]. For the influence of the transition time, the correction coefficient $x$ is provided by

$$x = \frac{\sum_{i=1}^{m} \Delta tdg\_b_i}{\sum_{i=1}^{m} \Delta tdg\_a_i}\,, \quad (19)$$

where Δ*tdg_a* is the delay time for the input signal of a rectangular wave, Δ*tdg_b* is the delay time for the input signal with a certain rising/falling time, and $m$ is the number of the changed threshold voltage of the MOS FET instead of aging.

For the influence of the fan-out number, the correction coefficient $y$ is provided by

$$y = \frac{\sum_{i=1}^{l} \Delta tdg\_c_i}{\sum_{i=1}^{l} \Delta tdg\_a_i}\,, \quad (20)$$

where Δ*tdg_c* is the delay time for the gate with a certain fan-out number and $l$ is the number of the changed threshold voltage of the MOS FET instead of aging.

Thus, the maximum increased delay time Δ*tdg* for each gate is calculated by

$$\Delta tdg = \Delta tsd \cdot w \cdot x \cdot y\,. \quad (21)$$

From the above, as the Δ*tdg* for each gate is obtained from the Δ*tsd* of one MOS FET, the maximum increased delay time of any path, Δ*tpd*, in the LSI chip is calculated by applying Δ*tdg* to gates on the path. For the estimation of Δ*tdg*, two approaches are considered. The first one calculates the path delay using the maximum increased delay time of the gate that does not consider its input value (method 1). The second one calculates the path delay considering the input value of the gate and the maximum value among *tpLH* or t*pHL* (method 2). In this work, we use both these methods in order to make the calculation as easy as possible.

## 5. Evaluation and considerations

In order to verify the effectiveness of the proposed methods, we carried out circuit simulations (HSpice) using 50-nm parameters [11]. The amount of aging is given by the increment of the threshold voltage, which was varied from 220 to 300 mV per 5-mV step. Table 1 shows the parameters of the MOS FET. The RO consists of 51 gates, the channel width of the NMOS-aged RO (NAND gate) is *Wp*/*Wn*=500 nm/500 nm and

*Wp*/*Wn*=2100 nm/500 nm for the PMOS-aged RO (NOR gate), and the channel length is *L*=50 nm.

Table 1 MOS FET parameters.

| Symbol | Value | | Unit |
|---|---|---|---|
| | NMOS | PMOS | |
| VDD | 1 | | V |
| Vth | 0.22 | -0.22 | V |
| μ0 | 0.032 | 0.0095 | $m^2/(V{\cdot}s)$ |
| δ1 | 0.001 | | - |
| Ua | $1.6\times10^{-10}$ | | m/V |
| Ub | $1.1\times10^{-17}$ | $8\times10^{-18}$ | $(m/V)^2$ |
| Uc | $-3\times10^{-11}$ | 4.6×10-13 | 1/V |
| Tox | $7\times10^{-10}$ | | m |
| K1 | 0.35 | 0.39 | - |
| K2 | 0.05 | 0.05 | - |
| KB | $1.3806488\times10^{-23}$ | | J/K |
| q | $1.602176565\times10^{-19}$ | | C |
| NDEP | $2.8\times10^{18}$ | | - |
| PHIN | 0 | | - |
| TNOM | 27 | | °C |

Figs. 6 and 7 show the increased delay times of one NMOS FET Δ*tsdn* and one PMOS FET Δ*tsdp*, respectively. The error rate of the Δ*tsdn* estimation was less than 0.13 ps (3.17%) and that of the Δ*tsdp* estimation was less than 0.083 ps (4.61%). This demonstrates that the proposed method can estimate the delay time of the MOS FET level within an error rate of 5 %. It seems the reason these error ratios are not constant is that the delay time of the MOS FET was calculated by the simplified RC circuit model.

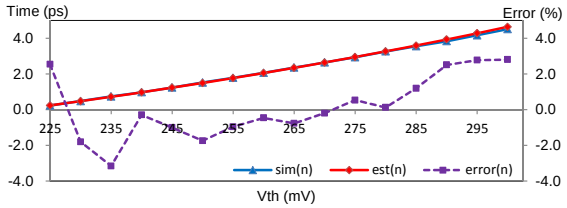



Figure 6 Δ*tsdn* estimation.

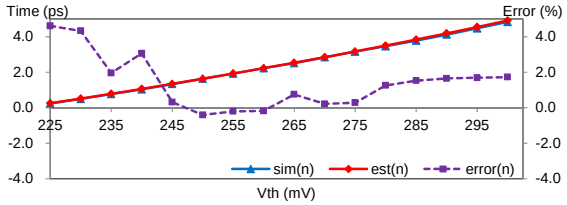



Figure 7 Δ*tsdp* estimation.

Table 2 shows the estimation results of $V_{th}$ calculated from (14), (15), and (17). Estimation error here refers to the difference between the $V_{th}$ obtained from the calculation and the $V_{th}$ used for simulation showing the same oscillation period $T_n$. MATLAB was used for solving Eq. (17). For the estimation of $V_{th}$ shift by aging, the proposed method can estimate the amount of $V_{th}$ shift within an error rate of 1 % at the MOS FET level. As the proposed estimation method uses the simple RC circuit model, there is an error for $V_{th}$ estimation. Estimation error of the $V_{thn}$ of the NMOS FET is less than 1.7 mv (0.57%), where $\Delta V_{thn}$=80 mV corresponds to the aging amount of the NMOS FET after 30 years and at that time there is an error of 400 days by the proposed estimation method for reaching the 80-mV increment (i.e., the time reaching to NMOS FET operating period for 80 mV increment is estimated as 28.9 years (=30-year - 400-day)). For PMOS FET, the estimation error of $V_{thp}$ is less than 1.1 mV (0.37 %). The model for calculating the estimation error of $V_{th}$ is based on [1].

Table 2 $V_{th}$ estimation.

| Vth (mV) | ΔVth (mV) | NMOS FET est. Vth (mV) | Error (mV) [(%)] | | Error (days) | PMOS FET est. Vth (mV) | Error (mV) [(%)] | | Error (days) |
|---|---|---|---|---|---|---|---|---|---|
| 225 | 5 | 224.90 | -0.10 | [-0.04] | -0.02/1 hr. | 224.80 | -0.20 | [-0.09] | -0.01/1 hr. |
| 230 | 10 | 230.20 | 0.20 | [0.09] | - | 229.60 | -0.40 | [-0.17] | - |
| 235 | 15 | 235.50 | 0.50 | [0.21] | - | 234.70 | -0.30 | [-0.13] | - |
| 240 | 20 | 240.10 | 0.10 | [0.04] | 3.68/1 yr. | 239.40 | -0.60 | [-0.25] | - |
| 245 | 25 | 245.20 | 0.20 | [0.08] | - | 244.90 | -0.10 | [-0.04] | - |
| 250 | 30 | 250.50 | 0.50 | [0.20] | - | 250.10 | 0.10 | [0.04] | 8.21/1 yr. |
| 255 | 35 | 255.30 | 0.30 | [0.12] | - | 255.10 | 0.10 | [0.04] | 31.66/5 yrs. |
| 260 | 40 | 260.20 | 0.20 | [0.08] | - | 260.10 | 0.10 | [0.04] | 56.63/10yrs. |
| 265 | 45 | 265.30 | 0.30 | [0.11] | 26.79/5 yrs. | 264.70 | -0.30 | [-0.11] | - |
| 270 | 50 | 270.10 | 0.10 | [0.04] | - | 269.90 | -0.10 | [-0.04] | -140.8/30 yrs. |
| 275 | 55 | 274.80 | -0.20 | [-0.07] | - | 274.90 | -0.10 | [-0.04] | - |
| 280 | 60 | 279.90 | -0.10 | [-0.04] | -13.00/10 yrs. | 279.40 | -0.60 | [-0.21] | - |
| 285 | 65 | 284.40 | -0.60 | [-0.21] | - | 284.20 | -0.80 | [-0.28] | - |
| 290 | 70 | 288.60 | -1.40 | [-0.48] | - | 289.00 | -1.00 | [-0.34] | - |
| 295 | 75 | 293.40 | -1.60 | [-0.54] | - | 294.00 | -1.00 | [-0.34] | - |
| 300 | 80 | 298.30 | -1.70 | [-0.57] | -400.0/30 yrs. | 298.90 | -1.10 | [-0.37] | - |

The method for estimating the path delay time is evaluated by using a two-bit adder consisting of two-input gates or three-input gates, which is a part of the standard logic circuit 74181. Fig. 8 shows the adder consisting of two-input gates. In the adder with three-input gates, the two-input gates in Fig. 8 are replaced with three-input ones. Table 3 shows the coefficients of *w*, *x*, and *y* used in (21).

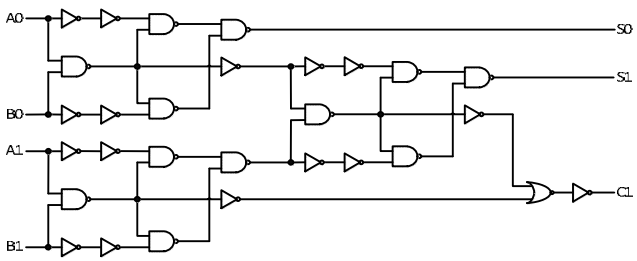



Figure 8 Two-bit adder (two-input gate).

Table 3 Conversion coefficients.

| | w | | x | y | |
|---|---|---|---|---|---|
| | tpHL | tpLH | | 2-fanout | 3-fanout |
| NOT | 0.81 | 0.89 | 1.6 | - | |
| 2NAND | 1.83 | 2.22 | 1.5 | 1.3 | 1.6 |
| 2NOR | 2.39 | 2.21 | 1.4 | - | |
| 3NAND | 2.73 | 4.35 | 1.3 | 1.3 | 1.6 |
| 3NOR | 3.43 | 3.32 | 1.7 | - | |

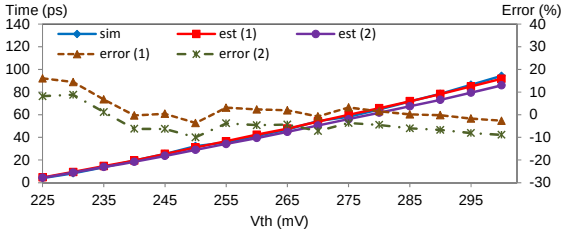



Figure 9 Delay time of B1-S1 path.

Fig. 9 shows the increased delay time, Δ*tpd*, of the path, B1-S1, containing the maximum number of gates. Table 4 summarizes the evaluation results for the estimation of the increased path delay time, where two kinds of paths are

selected: one with the maximum stage and the other with the maximum delay time. In method 1, the difference of the maximum increased delay time Δ*tpd* between the estimated value and the simulated one ranges from –12.27 ps to +33.87 ps (error from –16.11 % to +135.51 %). In method 2, it ranges from –20.28 ps to +8.99 ps (–22.71 % to +11.41 %).

Table 4 Summary of Δ*tpd*.

| Circuit | Path | Method 1 | | Method 2 | |
|---|---|---|---|---|---|
| | | Error (ps) | [(%)] | Error (ps) | [(%)] |
| 2-input adder | B0-S0 : max stage | 0.48 ~ 7.80 | [11.50 ~ 32.64] | 0.23 ~ 3.43 | [0.34 ~ 20.58] |
| | B1-S1 : max stage | -2.54 ~ 0.98 | [-3.68 ~ 16.06] | -8.35 ~ 0.33 | [-10.01 ~ 8.78] |
| | B1-C1 : max stage | -12.27 ~ -0.74 | [-16.11 ~ -2.58] | -20.28 ~ -1.45 | [-22.71 ~ -9.13] |
| | B0-S0 : max delay | -1.03 ~ 8.99 | [-25.97 ~ 23.88] | -1.22 ~ 5.30 | [-30.87 ~ 16.23] |
| | B1-S1 : max delay | 0.16 ~ 6.02 | [2.65 ~ 12.29] | -7.28 ~ -0.12 | [-9.09 ~ -0.32] |
| 3-input adder | B0-S0 : max stage | -0.12 ~ 12.21 | [-3.28 ~ 24.44] | -0.88 ~ 1.07 | [-21.13 ~ 5.64] |
| | B1-S1 : max stage | -1.35 ~ 11.18 | [-6.73 ~ 12.93] | -7.64 ~ 0.10 | [-18.84 ~ 1.66] |
| | B1-C1 : max stage | 0.86 ~ 12.93 | [6.73 ~ 17.41] | -6.59 ~ 1.07 | [-4.29 ~ 4.88] |
| | B0-S0 : max delay | 2.87 ~ 33.87 | [51.95 ~ 135.51] | 0.65 ~ 6.38 | [6.29 ~ 63.99] |
| | B1-S1 : max delay | 0.71 ~ 12.87 | [5.81 ~ 14.44] | 0.48 ~ 8.99 | [4.63 ~ 11.41] |

The reason the estimation result is higher than the simulation result is that the proposed method uses the maximum increased delay time of each gate. Conversely, the reason the estimation result is lower than the simulation result is that the load capacitance used by the calculation is smaller than that of the circuit used in the simulation.

Estimation results by method 1 are higher than those by method 2 because method 1 does not consider the input value and uses the maximum delay time of each gate while method 2 considers the input value and uses the maximum *tpHL* or *tpLH* and. Therefore, in many cases, the value of Δ*tpd* estimated by method 1 is higher than that by circuit simulation. In addition, the value of Δ*tpd* estimated by method 2 is close to that by circuit simulation.

Although we used two methods in this work for simple calculation, a more accurate estimation should be possible if an exact value applying to each gate, an exact gate size, and an exact load capacitance are used for calculation. However, the main purpose of this paper is to propose a method for estimating delay time with a reasonably good accuracy in as easy a manner as possible.

## 6. Conclusion

Our main objective in this work was to estimate the delay time increased by aging with a reasonably accurate method that can be applied as easily as possible. We therefore proposed an aging estimation method that uses two kinds of ROs to enable the switching delay time Δ*tsd* and the threshold voltage $\Delta V_{th}$ per MOS FET increased by aging to be estimated. The path delay time increased by aging is also estimated using these values. Results of evaluation within the aging amount range of 80 mV showed that Δ*tsd* can be estimated with an error rate of less than 0.13 ps and $\Delta V_{th}$ can be estimated with an error rate of less than 1.7 mV. For the path consisting of eight stage of a two-bit adder, Δ*tpd* can be estimated with an error rate of less than 20.28 ps.

In future work, we intend to develop a method incorporating the calculation of the load capacitance that considers circuit structure in order to elevate the estimation accuracy and an estimation method of the path delay time increased by real aging that considers the frequency of the gate usage.

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