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Short Paper

Layout Generator with Flexible Grid Assignment for Area Efficient Standard Cell

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Abstract: This paper discusses a standard cell layout generator that can be used to generate a standard cell library optimized to a target application. It can generate an area efficient layout from a virtual-grid symbolic layout with the ability of flexible grid positioning that considers local design rules enforced in a scaled technology. The generator reduces the cost of library design and enables an optimization of each cell with detailed layout information that can be used to estimate the performance of the cell under design. A standard cell library has been generated for commercial 28-nm FDSOI CMOS process using the proposed layout generator, and used for circuit design. Correct operation of designed circuit is observed form fabricated chip test.

Keywords: standard cell library, Computer-Aided Design, layout generator

1. Introduction

Standard cells are key building blocks for VLSI circuits, and its area, delay, and energy consumption have a strong impact on VLSI circuit performance. Since target performances are different by its design, standard cell library contains large amount of standard cells with different logic types and drive strengths. Usually, standard cells are carefully designed by designer, therefore building a large amount of standard cells requires large design cost.

Computer-Aided Design (CAD) tools for standard cell layout design are proposed to reduce the design cost of standard cell libraries. Device level synthesis has been proposed to generate optimal layout from schematic, considering optimal both geometrical placing and sizing of transistors and signal wires [1], [2]. Device level synthesis has a potential to generate optimal circuit layout, however, this technique has too much flexibility thus it is difficult for implementation. Also, this flexibility leads the difficulty of performance estimation at the circuit design phase.

On the other hand, the virtual grid symbolic layout has been proposed to generate optimal layout using dynamically generated cell library from process independent informations [3], [4], [5]. In this design methodology, cell library contains cell structure information as a template. This file contains the location of transistors and signal wires on a process independent virtual grid. Mask layout for each cell is generated from cell layout generator using the cell structure information and target process information. In this design methodology, a standard cell library for target process technology is generated from the layout generator, and used for circuit design. Therefore it is easy to use conventional CAD tools for library characterization, Place-and-Route, and performance prediction.

However, generated cell layout is restricted by its template cell structure information. To achieve area efficient cell layout design, the compaction of the symbolic layout is required for area efficient mask layout design [6]. Since symbolic layout requires conditional design rule and its depends on the mask layout design rules, it is difficult to develop the process portable symbolic layout. Also, on-current of both PMOS and NMOS transistors are also different by its process technology therefore optimal transistor width depend on the process technology.

To solve this problem, we developed a cell layout generator with flexible track assignment from symbolic layout to mask layout. This generator have a ability to generate different cell layouts with different P/N-well boundary and internal metal wiring from a same symbolic layout. This ability achieves both area efficient cell layout design and higher process portability of symbolic layout design. **Figure 1** shows an example of the limitation of the symbolic layout based cell library generation. Compare to the optimal cell, generated cell becomes less area efficiency.

Lowering the supply voltage has a significant impact on the energy reduction of the circuits. However, lowering the supply voltage increases not only the delay of standard cells, but also the imbalance of rise and fall delays of multi-input cells. Transistor width optimization and PMOS/NMOS ratio (P/N ratio) optimization are able to reduce this imbalance of the rise and fall delays of standard cells [7], [8]. However, parasitic RC inside a standard cell have a large impact on standard cell performance and this parasitic RC strongly depends on its cell layout. Standard cell layouts are required for accurate evaluation and exploration

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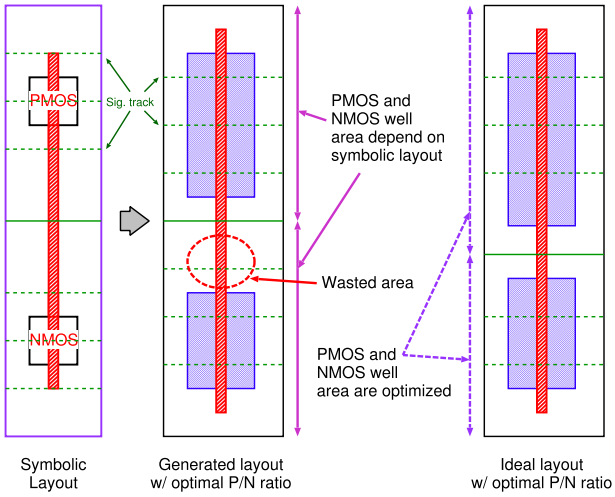

Fig. 1 Comparison between symbolic layout based cell layout and ideal layout.

of transistor width optimization for both energy and delay reduction.

In this paper, we discuss our developed standard cell layout generator. Our layout generator uses symbolic layout as a process independent cell layout structure information, and generate process dependent mask layout using process technology mapping. Our layout generator supports generating standard cell library with flexible P/N well boundaries and flexible wire track assignment for transistor width optimization with high area efficiency.

This flexibility can be used to balance P/N on-current ratio, and achieves optimal delay and energy performance at specific technology and supply voltage. Also, standard cells with flexible P/N well boundaries are able to optimize P/N on-current ratio of each cell, individually. We generated standard cell library for commercial 28-nm CMOS technology using this proposed standard cell layout generator. This standard cell library used for building a control logic of our test circuit using commercial Place-and-Route tool. The fabricated test chip works correctly at the functional testing.

The rest of this paper is organized as follows. Section 2 describes the layout generation tool. Section 3 discusses the generation results of standard cell library. Section 4 concludes this paper.

2. Layout Generator with Flexible Grid Assignment

In this section, we describe our developed standard cell layout generator. **Figure 2** shows the cell layout optimization flow of our layout generator. The layout generator discussed in this paper is used for the cell layout generation from a symbolic layout and several constraint informations. This layout generator generates standard cell layout with flexible horizontal grid assignment. This layout generator is developed not only for the cell layout generation, but also for the cell layout optimization. For the use of the cell layout optimization, optimization routine runs the cell layout generator to generates several standard cells with different transistor sizes. Optimization routine evaluates these performance and find the optimal transistor sizes for each standard cell.

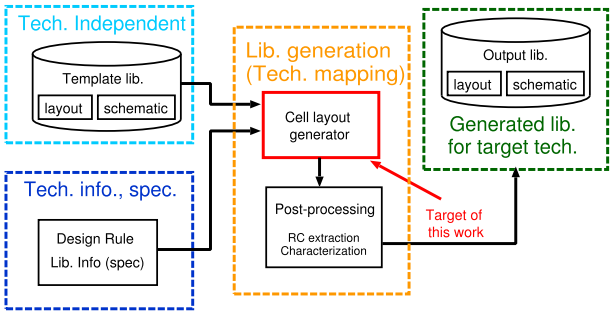

Fig. 2 Cell layout generation flow with developed layout generator.

2.1 Input Files

In this section, the input files of the developed layout generator are described. Developed layout generator uses symbolic layout based layout generation. Process independent template layout is mapped to process dependent layout using mask design rule and target library information.

Symbolic Layout

Symbolic layout is a process independent layout, which describes the circuit topology of the target cell. The symbolic layout contains the circuit components (e.g., MOS transistors, metal wires, contacts) which are called symbolic objects. The symbolic layout defines the location information of these symbolic objects on a process independent virtual grid. These circuit components are called Symbolic Objects.

Mask Design Rule

Mask design rule is the technology file and it describes design rules of target process technology. This file should contain width, length and spacing information of each mask layer object.

Target Library Information

The target library information contains the common specifications of generated library. Unit Tile size, cell height pitch, power rail metal layers and metal width are described.

2.2 Virtual Grid and Mask Layout Grid

In symbolic layout based layout generation, each symbolic object is placed on the virtual grid. The mask layout grid is calculated using mask design rules and target library information file. Layout generator map symbolic objects to the corresponding mask grid, and converts symbolic objects to the set of mask layers.

2.2.1 Virtual Grid for Symbolic Objects

Virtual Grid is used to define the placement coordinate of each symbolic object. To reduce the complexity of symbolic object placement, placement restrictions are introduced. The x-axis placement grid is called GridX. X-axis metal placement grid (Metal GridX) and x-axis PMOS/NMOS placement grid (Poly GridX) are alternately mapped on GridX. Metal GridX is used for the placement of the vertical metal wires between two transistors, and diffusion access contacts. Poly GridX is used for the placement of the PMOS/NMOS, the vertical metal wires over the transistors, and poly access contacts. GridY correspond to the horizontal wire track. Definition of GridX and GridY is illustrated in **Fig. 3**.

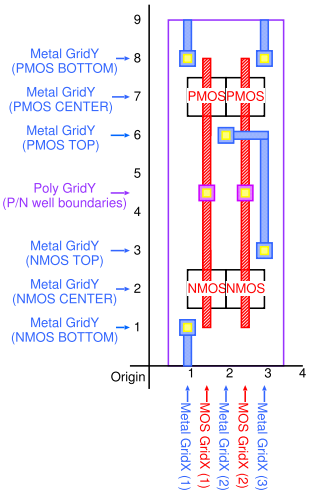

Fig. 3 Virtual grid of symbolic layout for symbolic object placement.

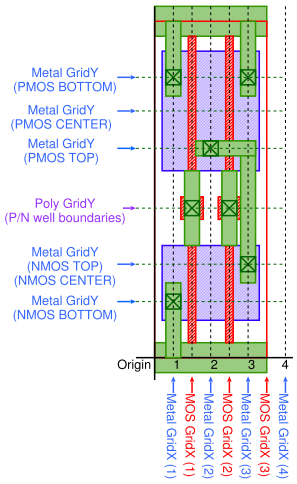

Fig. 4 Example illustration of the generated mask layout (PMOS 3 grid, NMOS 2 grid).

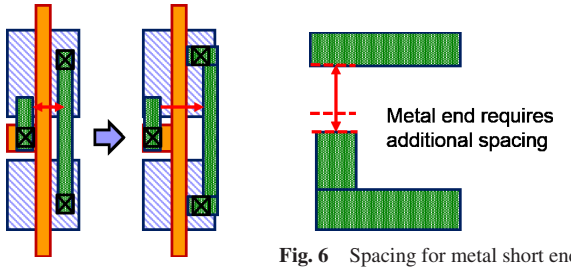

Fig. 5 Off-grid processing on layout.

Fig. 6 Spacing for metal short end.

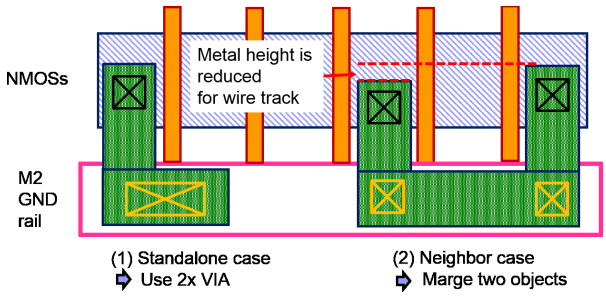

Fig. 7 Power supply path optimizations for signal resources.

2.2.2 Mask Layout Grid for Mask Layout

The mask layout grid is calculated using mask design rule and target library information to map the coordinate of symbolic objects to set of mask layouts. GridX of the virtual grid correspond to the contacted pitch of diffusion access contacts on symbolic layout, therefore GridX of the mask layout grid is converted to contacted pitch of diffusion access contacts on mask layout. In case of the diffusion break at layout, corresponding GridX is locally updated and settled to the minimum distance of two contacts with diffusion break.

GridY of virtual grid and mask layout grid correspond to the horizontal wire track of the symbolic layout and the mask layout, respectively. Since the available number of horizontal wire track on the mask layout depend on the PMOS and NMOS width and it is affected by mask design rule and target cell height, GridY of virtual grid is not able to directly converse to the mask layout grid. In case of the mismatch of the number of horizontal track, developed layout generator merge some GridY of virtual grid, and mapped to corresponding mask layout.

Figure 4 shows the illustration of translated NAND2 cell and mask layout grid. In this case, there are only two GridY tracks are available on NMOS region, thus "NMOS CENTER" and "NMOS TOP" on symbolic grid are merged.

2.3 Exception Handling on Layout Generation

Direct mapping of a symbolic layout to mask layout will violate a design rule, since there are many exceptions and complex conditions in design rules, especially deeply scaled process technology. Several exception handling procedures are implemented in the layout generator to handle this complex design rules.

Off Grid Placement

If contacted pitch is not larger than twice of metal track pitch, the space of the MOS GridX and the Metal GridX becomes thinner than minimum metal wire pitch and it may cause the design rule violation. To ensure the clearance of two metals, off-grid function detects this violation and move both metals and related objects to fix the violation (**Fig. 5**).

Additional Space for Metal Short Side

Generally, there are many conditions and variations of the minimum space rule on process technology. In some process, additional space is required for narrow object layers. In case of the requirement, developed generator has a function to detect and fix the metal short side space rule (**Fig. 6**).

Flexibility of the Power Rail

Developed layout generator support for generating the power rail using both Metal 1 layer type and Metal 2 layer type with arbitrary metal width. For the Metal 2 power rail structure, Metal 1 wire and VIAs are used to connect the power rail and the transistor source. Number of VIAs for power are automatically merged to maximize the resources for the local metal signals. The shape of the metal surroundings for the VIA is also optimized to maximize metal area (**Fig. 7**).

2.4 Output Files

We make out layout generator to output the cell layouts as a Cadence SKILL language, and corresponding schematics as a CDL format. Cadence Virtuoso is used for the cell layout construction using SKILL language.

3. Experimental Results of Layout Generation

3.1 Layout Generation Example

We developed standard cell library for commercial 28-nm FD-SOI CMOS process. This standard cell library has a 9-Grid cell height, and Metal 2 power rail. The developed standard cell library contains Inverter, Buffer, NAND2,4, NOR2,4, AOI21, OAI21, and Filler cells with different drive strength. D-Flip-Flop and TAP cell are manually designed and used in this library. **Table 1** summarizes the generated cells.

Figure 8 shows the symbolic layout of NAND2 cell, and **Fig. 9** shows the generated NAND2 cell mask layout. Result shows library generator can generate standard cell layout which satisfy the design rule. In this design, both cell width and transistors width are almost same between the generated cell and the man-

Table 1 List of generated standard cells.

Cell Type	Strength
Inverter	1.0x 1.5x 2.0x 3.0x 4.0x 8.0x 16.0x
Buffer	1.0x 1.5x 2.0x 3.0x 4.0x 8.0x 16.0x
NAND2	1.0x 2.0x 4.0x 8.0x
NAND4	1.0x 2.0x 4.0x
NOR2	1.0x 2.0x 4.0x 8.0x
NOR4	1.0x 2.0x 4.0x
AOI21	1.0x 2.0x
OAI21	1.0x 2.0x
FILL	1.0 2.0 4.0
FILL (Capacitance)	22.0x

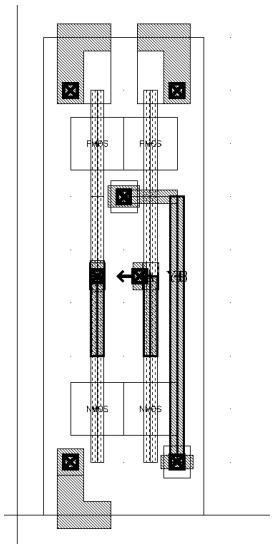

Fig. 8 Symbolic layout of NAND2 cell.

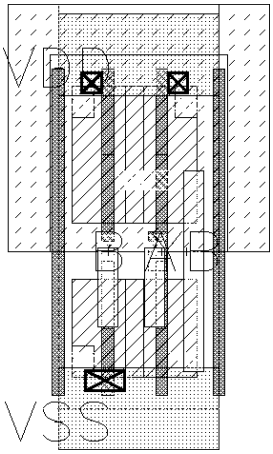

Fig. 9 Generated NAND2 mask layout.

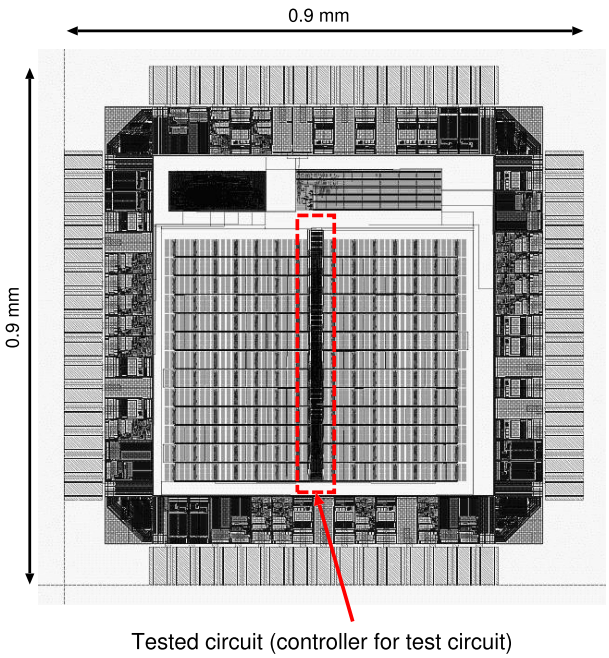

Fig. 10 Layout of fabricated test chip.

ually designed cell. Area efficiency of generated cell is almost equivalent to the manually designed cell.

3.2 Implementation on Real Silicon

Generated standard cell library is characterized and used for building the control logic of test circuit using synthesis and automated Place-and-Route. **Figure 10** shows the chip layout. Fabricated test chip has been tested, and the test result shows the control logic circuits with generated standard cell works correctly.

4. Conclusion

In this paper, we describe our developed standard cell layout generator. This layout generator has a flexibility for the location of the P/N well boundaries, and for the horizontal wire track assignment. This flexibility achieves area efficient layout generation. This layout generator is used for a standard cell library generation which targets consumer 28-nm FDSOI CMOS process.

Our future work is measurement and evaluation of the standard cell delay performance on real silicon, which is implemented as Ring Oscillator circuits. Improvement of layout flexibility of standard cell is still required for the generation of complex cells, such as D-Flip-Flops and MUXs. More detailed comparison of the standard cell libraries designed with our layout generator design and manual design is also planned using benchmark circuits design. Also, we are planning the implementation of transistor width optimization flow utilizing developed layout generator.

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References

[1] Liu, C.P.L. and Abraham, J.A.: Transistor Level Synthesis for Static CMOS Combinational Circuits, *Great Lakes Symposium on VLSI*, pp.172–175 (1999).
[2] Kagaris, D. and Haniotakis, T.: Transistor-Level Synthesis for Low-Power Applications, *International Symposium on Quality Electronic Design*, pp.607–612 (2007).
[3] Burns, J.L. and Feldman, J.A.: C5M-a control-logic layout synthesis system for high-performance microprocessors, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.17, No.1, pp.14–23 (1998).
[4] Onodera, H., Hashimoto, M. and Hashimoto, T.: ASIC design methodology with on-demand library generation, *Symposium on VLSI Circuits*, pp.57–60, Japan Soc. Appl. Phys. (2001).
[5] Hashimoto, M., Fujimori, K. and Onodera, H.: Automatic Generation of Standard Cell Library in VDSM Technologies 2 Layout generation system: VARDS, *International Symposium on Quality Electronic Design*, pp.36–41 (2004).
[6] Cheng, C.K., Deng, X., Liao, Y.Z. and Yao, S.Z.: Symbolic Layout Compaction Under Conditional Design Rules, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.11, No.April, pp.475–486 (1992).
[7] Kung, D.S. and Puri, R.: Optimal P/N width ratio selection for standard cell libraries, *International Conference on Computer-Aided Design*, pp.178–184 (1999).
[8] Nishizawa, S., Ishihara, T. and Onodera, H.: A Flexible Structure of Standard Cell and Its Optimization Method for Near-Threshold Voltage Operation, *International Conference on Computer Design*, pp.235–240 (2012).

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