A Note on Efficient Layouts for de Bruijn Networks *

4 C − 4

Yoshiyasu Doi, Toshinori Yamada, and Shuichi Ueno †
Department of Physical Electronics, Tokyo Institute of Technology ‡

Abstract

This note shows a simple and efficient layout of the de Bruijn network, and proposes a fault-tolerant de Bruijn network with an area-optimal layout.

1 Networks

$\{0,1\}^n$ is the set of binary strings of length n, and $\overline{x}$ is the binary complement of $x \in \{0,1\}$. We define two bijections on $\{0,1\}^n$ as follows:

$$\begin{aligned} \sigma(v_0v_1\ldots v_{n-1}) &= v_1\ldots v_{n-1}v_0 \\ \chi(v_0v_1\ldots v_{n-1}) &= v_0v_1\ldots \overline{v}_{n-1}. \end{aligned}$$

We define six more bijections which are composites of σ and χ as follows:

$$\begin{aligned} f_1(v_0v_1\ldots v_{n-1}) &= v_1\ldots v_{n-1}\overline{v}_0 \\ f_2(v_0v_1\ldots v_{n-1}) &= v_1\ldots \overline{v}_{n-1}v_0 \\ f_3(v_0v_1v_2\ldots v_{n-1}) &= v_2\ldots v_{n-1}v_0v_1 \\ f_4(v_0v_1v_2\ldots v_{n-1}) &= v_2\ldots v_{n-1}\overline{v}_0v_1 \\ f_5(v_0v_1\ldots v_{n-1}) &= v_1\ldots \overline{v}_{n-1}\overline{v}_0 \\ f_6(v_0v_1v_2\ldots v_{n-1}) &= v_2\ldots v_{n-1}\overline{v}_0\overline{v}_1. \end{aligned}$$

Notice that $f_1 = \chi\cdot\sigma$, $f_2 = \sigma\cdot\chi$, $f_3 = \sigma\cdot\sigma$, $f_4 = \sigma\cdot\chi\cdot\sigma$, $f_5 = \chi\cdot\sigma\cdot\chi$, and $f_6 = \chi\cdot\sigma\cdot\chi\cdot\sigma$.

The shuffle-exchange network of dimention n, denoted by $SX(n)$, is the graph such that the vertex set is $\{0,1\}^n$ and for any vertex v, each of $\sigma(v)$, $\sigma^{-1}(v)$, and $\chi(v)$ is connected with v by an edge. The de Bruijn network of dimension n, denoted by $dB(n)$, is the graph such that the vertex set is $\{0,1\}^n$ and for any vertex v, each of $\sigma(v)$, $\sigma^{-1}(v)$, $f_1(v)$, and $f_1^{-1}(v)$ is connected with v by an edge. $SX(3)$ and $dB(3)$ are shown in Figures 1 and 2, respectively.

It is easy to see that $SX(n)$ is a subgraph of $dB(n)$. The edges $(v,\sigma(v))$, $(v,\chi(v))$, and $(v,f_1(v))$ are called an σ-edge, χ-edge, and f_1-edge, respectively. In Figures 1 and 2, σ-edges are shown with solid lines. Dashed lines are χ-edges and f_1-edges in Figures 1 and 2, respectively. A necklace is a cycle consisting of σ-edges. It is easy to see that the vertices of $SX(n)$ and $dB(n)$ can be partitioned into necklaces.

2 Layouts

Leighton showed that $SX(n)$ can be laid out in optimal area of $\Theta(N^2/\log^2 N)$, where $N = 2^n$ is the number of vertices of $SX(n)$ [2]. The layout is obtained by linearly arranging the necklaces. Samatham and Pradhan proposed a procedure to lay out $dB(n)$ in optimal area using the layout of $SX(n+1)$ by Leighton [3]. They showed that if the layout of $SX(n)$ has area A then their layout of $dB(n)$ has area at most $16A$.

We show a simple procedure to lay out $dB(n)$ in less area using the layout of $SX(n)$ by Leighton. Our procedure is summarized in the following algorithm. A key idea behind our procedure is a simple fact that $dB(n)$ can be embedded into $SX(n)$ with both dilation and congestion 2.

Algorithm 1

Step1: Lay out $SX(n)$ by an algorithm in [2].

Step2: Double the lengths and widths of all vertices and edges, so each vertex occupies a 2×2 area and double the length of all edges.

Step3: Duplicate each edge.

Step4: For each vertex v, concatenate σ-edge $(\sigma^{-1}(v), v)$ and χ-edge $(v,\chi(v))$ to form f_1-edge $(\sigma^{-1}(v),\chi(v))$. ■

Layouts of $SX(3)$ and $dB(3)$ are shown in Figures 3 and 4, respectively. We can show the following.

Theorem 1 *If the layout of $SX(n)$ has area A then our layout of $dB(n)$ has area at most $4A$.* ■

*de Bruijn ネットワークの効率的なレイアウトについて
†土肥 義康, 山田 敏規, 上野 修一
‡東京工業大学 電子物理工学科

3 Fault-Tolerant Networks

A graph G is called a t-fault-tolerant graph for a graph H if even after removing any t vertices from G, the remaining graph contains H as a subgraph. Bruck, Cypher, and Ho showed a t-fault-tolerant graph for $dB(n)$ with small vertex degree [1]. However, no efficient layout of the t-fault-tolerant graph is known even for the case of $t = 1$. We propose a new 1-fault-tolerant graph for $dB(n)$ with an area-optimal layout.

Let $G(n)$ be a graph obtained from $dB(n)$ by adding edges so that for any vertex v, each of $\sigma(v)$, $\sigma^{-1}(v)$, $\chi(v)$, $f_1(v)$, $f_1^{-1}(v)$, $f_2(v)$, $f_2^{-1}(v)$, $f_3(v)$, $f_3^{-1}(v)$, $f_4(v)$, $f_4^{-1}(v)$, $f_5(v)$, $f_5^{-1}(v)$, $f_6(v)$, and $f_6^{-1}(v)$ is connected with v by an edge. Let $FT(n)$ be a graph obtained from $G(n)$ by adding a vertex u and edges so that each of the neighbors of 0^n in $G(n)$ is connected with u by an edge. We can prove the following.

Theorem 2 *$FT(n)$ is a 1-fault-tolerant graph for $dB(n)$. Moreover, if our layout of $dB(n)$ has area A' then $FT(n)$ can be laid out in area of $42A'$.* ■

Acknowledgments: The authors are grateful to Prof.Y.Kajitani for his encouragement. The research is a part of CAD21 Project at TIT.

References

[1] J.Bruck, R.Cypher, and C.-T. Ho. Fault-tolerant de Bruijn and shuffle-exchange networks. *IEEE Trans. on Parallel and Distributed Systems*, Vol. 5, No. 5, pp. 548–553, 1994.

[2] F.T. Leighton. *Complexity Issue in VLSI: Optimal Layout for the Shuffle-Exchange Graph and Other Networks.* Foundations of Computing. The Mit Press, 1983.

[3] M.R.Samatham and D.K.Pradhan. The de Bruijn multiprocessor network: A versatile parallel processing and sorting network for VLSI. *IEEE Trans. on Computers*, Vol. 38, No. 4, pp. 567–581, 1989.

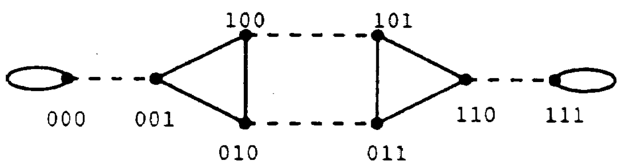

Figure 1: SX(3)

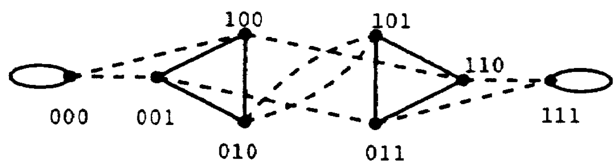

Figure 2: dB(3)

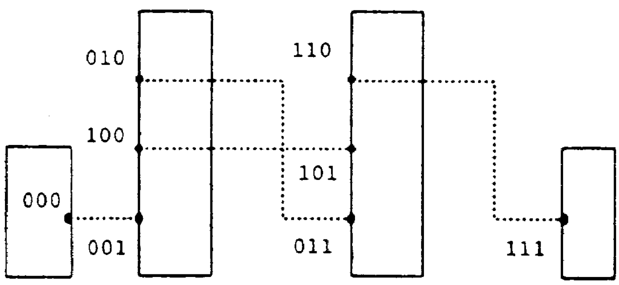

Figure 3: Layout for SX(3)

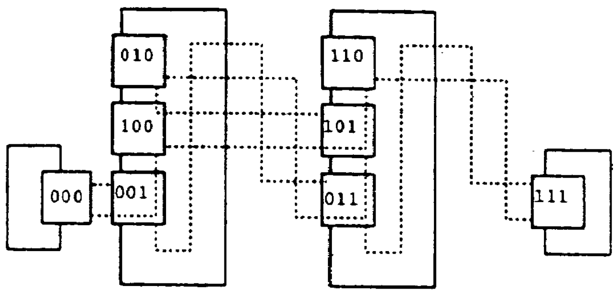

Figure 4: Layout for dB(3)