On H1SL Faults Covered by Multiple Times Detection Test Set for SSA Faults

2R－8

Junzhi Sang Haruhiko Takase Terumine Hayashi
Department of Electrical and Electronic Engineering, Faculty of Engineering, Mie University
1515 Kamihama-cho, Tsu 514-8507, Japan
E-mail: {sang, takase, hayashi}@hayashi.elec.mie-u.ac.jp

1. Introduction

Although *single stuck-at fault* (SSAF) model does not cover all static defects in digital circuits, it is still widely used now. It is due to the following reasons: (1) the test set with 100% SSAF coverage can detect many other static defects, (2) the SSAF test set is acceptable in detecting actual defects, and SSAF coverage is considered as an appropriate measure for evaluating the quality of a test set, and (3) SSAF model can be easily implemented in CAD systems, for the number of SSAFs is in proportion to that of gates in a circuit. Recently, with the development of IC technology, the insufficiency of SSAF model is frequently pointed out. Suspicion is falling upon the ability of SSAF model as the most common fault model. To compensate for this, some methods like adopting other fault models as complementary (or substitutive) models to the SSAF model were recommended. Although more defects could be detected by adopting other fault models, the load of CAD system and tester may increase by a large amount of faults and test vectors. For example, the number of bridging faults is proportional of the signal line number to the power of 2 in a chip.

In this paper, a new fault model, called *single logical fault with Hamming distance 1* (H1SLF) is proposed. The amount of H1SLFs is roughly equal to that of SSAFs in a circuit, but the new model is possible to cover more defects than SSAF model. We present some experimental results on H1SLFs covered by multiple times detection test set for SSAFs to demonstrate the effectiveness of H1SLF model.

2. H1SLF Model

In this section, we introduce the definition of H1SLF model, and compare it with SSAF model and *single logical fault* (SLF) model, under the single-fault assumption.

Consider a gate G with k input pins $I_1, I_2, \ldots, I_k$, with input values $a_1, a_2, \ldots, a_k$, and output value $v(p)$. Here, $p = \sum_{i=1}^{k} a_i \cdot 2^{i-1}$. A *behavior vector* of the gate is defined as a vector of output values ($v(0)$, $v(1)$, ..., $v(2^k-1)$). The behavior vector of fault-free gate is called *good behavior vector* (GBV), and that of faulty gate is called *faulty behavior vector* (FBV). The number of FBVs of the gate is equal to $2^{2^k}-1$, because the behavior vectors of the gate are all combinations of 2^k elements. Each FBV corresponds to a SLF. In SLFs, those faults whose FBVs are different from GBV in only one element $v(p)$ of behavior vector are called H1SLF and denoted as $F(G,p)$. The number of H1SLFs of the gate is equal to 2^k. Table 1 shows the fault relation among SLF, H1SLF and SSAF in an AND gate G with 2 input pins. GM corresponds to the GBV (0,0,0,1) of the gate.

In general, the following properties can be easily concluded from the characteristic of SSAF model, SLF model and H1SLF model.

Property 1: The set of SLFs covers that of SSAFs, and

Table 1. Faults in a AND Gate G with 2 Input Pins

gate behavior vector v(0)	v(1)	v(2)	v(3)	SLF	H1SLF	SSAF
0	0	0	0	F0	F(G, 3)	s.a.0 at output
1	0	0	0	F1		
0	1	0	0	F2		
1	1	0	0	F3		
0	0	1	0	F4		
1	0	1	0	F5		
0	1	1	0	F6		
1	1	1	0	F7		
0	0	0	1	GM	GM	GM
1	0	0	1	F9	F(G, 0)	
0	1	0	1	F10	F(G, 1)	s.a.1 at input 2
1	1	0	1	F11		
0	0	1	1	F12	F(G, 2)	s.a.1 at input 1
1	0	1	1	F13		
0	1	1	1	F14		
1	1	1	1	F15		s.a.1 at output

Table 2. The Number of Faults in Each Fault Model

circuit	#SSAF	#H1SLF	#SLF	#SBF
c432	524	2466	$4.0*10^{154}$	19110
c499	758	1050	$3.4*10^{10}$	29403
c880	942	1377	862273	97903
c1355	1574	2122	$3.4*10^{10}$	171991
c1908	1879	4709	$7.0*10^{77}$	416328
c2670	2747	4166	$3.9*10^{10}$	1016025
c3540	3428	8791	$1.9*10^{78}$	1476621
c5315	5350	10011	$2.7*10^{154}$	3086370
c6288	7744	8688	34032	2995128
c7552	7550	11860	$2.4*10^{11}$	6913621

also covers that of H1SLFs in a circuit.

Property 2: A test set which detects all detectable H1SLFs, can detect all detectable SLFs, and also can detect all detectable SSAFs in a circuit.

From the above properties, H1SLF model seems to have the same ability on defect coverage as SLF model, and a powerful defect coverage over SSAF model. As shown in Table 2, the number of H1SLFs is the same order as that of SSAFs, and is much less than that of SLFs or *single bridging faults* (SBF) in a circuit. Here, the numbers of H1SLFs in Table 2 are the sizes of H1SLF sets after collapsing equivalent faults , as SSAF model.

3. H1SLFs Covered by Test Set for SSAFs

First, we use the real-valued logic simulation [1] to generate our original multi-detection test sets. The method is based on an iterative improvement method, and easy to generate multi-detection test sets by changing its initial seed. Next, we compact the original test sets by the methods of extracting essential test patterns and reverse order simulation. Then, the undetected H1SLFs for the compacted test sets are computed by a H1SLF simulator.

As shown in Table 3, we repeated the experiment for each circuit of ISCAS'85, in the condition of 1, 2, 5, 10 time(s) SSAF detection separately. Each test set can detect all detectable SSAFs *n* time(s). We list the numbers of test patterns and the numbers of undetected H1SLFs (not including redundant faults) in Table 3. However, we cannot draw the similar conclusion as in [2], from the experimental results. [2] shows that a test set generated for SSAF n-detection covers most of SBFs, and its fault coverage achieves nearly 99.9% (including redundant bridging faults) in most of cases. Although more H1SLFs can be detected by increasing SSAF detection times, there are still a considerable undetected H1SLFs left.

4. H1SLF Test Set Generation

It is easy to convert an SSAF test generator to a H1SLF test generator. We modified the above test generator and generate test sets for H1SLFs. Table 4 shows the results of the experiments. Test sets in Table 4 can detect all detectable H1SLFs and can cover all detectable SSAFs for corresponding circuits. It shows that the test generation for H1SLFs is more effective than that for SSAFs.

5. Concluding Remarks

We proposed a new fault model of H1SLF. Although the amount of H1SLFs is roughly equal to that of SSAFs in a circuit, H1SLF model is possible to cover more defects than SSAF model. Our experimental results show that many detectable H1SLFs cannot be detected by a n-detection test set for SSAFs, even *n* is set to 10. But the test set generated for H1SLFs can cover all SSAFs. That is to say, the test generation for H1SLFs is more effective than that for SSAF multiple detection.

In the future, we will continue to study the other aspects of H1SLF model, as in computing the minimal test set, the SBF coverage by a H1SLF test set, and a better test generator.

References

[1] K. Hatayama, K. Hikone, M. Ikeda and T. Hayashi: "Sequential Test Generation Based on Real-Valued Logic Simulation," Int'l Test Conference, 1992.

[2] S. M. Reddy, I. Pomeranz and S. Kajihara: "On the Effects of Test Compaction on Defect Coverage," Proc. 14th VLSI Test Symp., 1996.

Table 3 . H1SLFs Detected by Multi-detection Test Sets for SSAFs

circuit	1-detection		2-detection		5-detection		10-detection	
	tp	udf (fc)	tp	udf (fc)	tp	udf (fc)	tp	udf (fc)
c432	53	1772 (25.8)	96	1716(28.1)	236	1629(31.8)	460	1542(35.4)
c499	54	152 (84.7)	104	135(86.4)	260	121(87.8)	520	120(87.9)
c880	57	118 (90.7)	86	103(91.9)	216	50(96.0)	410	36(97.1)
c1355	85	120 (92.7)	168	120(92.7)	421	120(92.7)	840	120(92.7)
c1908	123	421 (86.4)	232	368(88.1)	591	289(90.7)	1175	259(91.6)
c2670	105	215 (93.5)	188	178(94.6)	426	127(96.1)	831	103(96.9)
c3540	154	114 (97.0)	284	92(97.6)	638	65(98.3)	1221	52(98.6)
c5315	115	1106 (86.3)	204	815(89.5)	443	552(93.2)	868	296(96.3)
c6288	33	22 (99.6)	46	5(99.9)	86	2(99.9)	156	0(100)
c7552	180	521 (94.3)	345	346(96.2)	793	215(97.6)	1551	147(98.4)

tp: the number of test patterns for SSAF n-detection
udf: the number of undetected H1SLFs
fc: H1SLF coverage, ⌊(#detected H1SLF / #detectable H1SLF)*1000⌋/10

Table 4 . Test Sets for 100% H1SLF Coverage

circuit	tp
c432	943
c499	104
c880	112
c1355	105
c1908	336
c2670	211
c3540	215
c5315	628
c6288	34
c7552	337