Invited Paper

Advances in PCB Routing

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Abstract: The increasing complexity of electronic systems has made PCB routing a difficult problem. A large amount of research effort has been dedicated to the study of this problem. In this paper, we provide an overview of recent research results on the PCB routing problem. We focus on the escape routing problem and the length-matching routing problem, which are the two most important problems in PCB routing. Other relevant works are also briefly introduced.

Keywords: PCB routing, escape routing, length-matching routing, network-flow

1. Introduction

The constantly evolving manufacturing technology continues to push the complexity of integrated circuits to new heights. For example, the new Intel Core i7 contains more than 1 billion transistors. A direct result of this exploding complexity is the dramatic increase in the complexity of packages and printed circuit boards (PCBs). Today's high-end packages can have over 2,000 pins [1]. A typical high-end PCB could have more than 10,000 signal nets. On the other hand, the size of a package is kept to a minimum, making the footprint of such a package on a PCB a very dense pin grid.

Such a large net count and high pin density make manual design of PCBs an extremely time consuming and error-prone task. Furthermore, the increasing clock frequency imposes special physical constraints such as length-matching routing, pairwise routing, planar routing, etc., on high-performance PCBs [2], [3], [4], [5]. These constraints make traditional IC and PCB routers not applicable to modern PCB routing. To the best of our knowledge, there is no mature commercial automated router that handles these constraints well. Therefore, automated PCB routers that are tuned to handle such constraints are in great demand for modern high-performance PCB layout. Because of such demand, a tremendous amount of research has focused on PCB routing problems in recent years. Two major topics in PCB routing are escape routing and length-matching routing. In this paper, we give an overview of recent research efforts on these two topics. The rest of this paper is organized as follows: Section 2 gives some background about the PCB routing problem. In Section 3, we introduce recent research advances on escape routing. In Section 4, we introduce the projection based escape routing style and provide a study of its related bus escape planning problem. Then in Section 5, we survey the research results on length-matching routing. In the last Section, we briefly cover the research results in some other relevant topics.

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2. PCB Routing Problem

A modern PCB usually hosts several chip packages whose footprints are arrays of pins (see **Fig. 1**). Such pin arrays are expected to be connected by non-crossing wires. Not all connections can be routed on one layer, so multiple layers are used to accommodate all the wire connections. However, introducing vias at the middle of a route would introduce reflection and ringing effects which can cause serious signal integrity issues [4], [5]. Therefore, it is highly preferred that no vias are inserted in the middle of the routing (vias are allowed at the two ends to connect to the package pin/ball). This requires the routing of a signal net to be planar without switching layers in the middle. This planar routing style makes PCB routing very different from IC routing, which uses conventional XY routing style with a preferred routing direction for each routing layer. Therefore, conventional IC routing algorithms cannot be used to solve the PCB routing problem.

There are two important problems in PCB routing:

(1) **Escape routing**: route from pins inside the pin arrays to the boundary of the arrays (help the pins "escape" the pin array).

(2) **Length-matching routing**: connect the escaped routes between the pin arrays while satisfying stringent length constraints.

Escape routing and length-matching routing have different tasks. Since escape routing usually dominates the total number of layers, its major task is to escape a set of pins using as few layers as possible. Sometimes it may also need to provide matching net orderings along the boundaries of the two arrays in order to provide a planar topology for later length-matching routing. The focus of length-matching routing, on the other hand, is to carefully detour the wires to meet the length constraints while maintaining the planar topology inherited from escape routing.

3. Escape Routing

Among all the PCB routing problems, escape routing is probably the most intensively studied. It can be further classified into three categories:
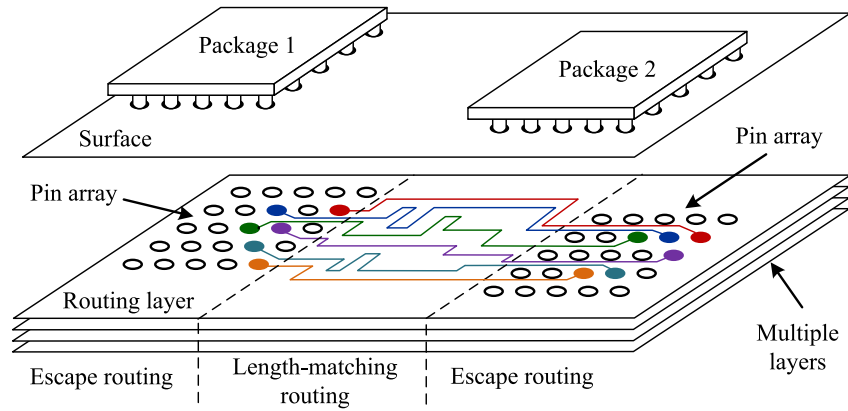
Fig. 1   An illustration of PCB routing.

(a) Flow model for a pin grid   (b) Inside a tile
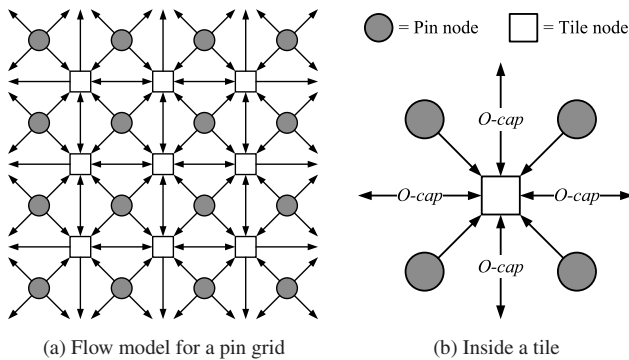
Fig. 2   Typical network-flow model for unordered escape routing problem.

Fig. 3   Yan and Wong's [11] network-flow model inside a tile.

- **Unordered escape** is to route from the pins inside a pin array to the boundary of the array without any constraint on the pin ordering along the boundary.
- **Ordered escape** also considers only one pin array. However, it requires the escape routing to conform to a specified ordering along the boundary.
- **Simultaneous escape** considers escape routing of two pin arrays. The ordering of the escaped routes in the two arrays are required to match in order to provide a planar topology for later length-matching routing.

The three types of escape routing problems all have applications in PCB routing.

Both unordered and ordered escape routing problems involve only a single pin array. Studies of these problems are undertaken not only within PCB routing research but also within package routing research because package designers also face the problem of routing from inside a pin array to some linearly arranged bonding pads. Simultaneous escape routing, however, is only for PCB routing.

3.1   Unordered Escape

Network-flow approaches are pervasively used to solve the unordered escape routing problem. The idea is to view each routing path as a unit flow from the pin to the boundary. Since no ordering is specified, a flow solution always corresponds to some non-crossing routing. A typical network model looks like **Fig. 2**. Representative works using network-flow to solve the unordered problem include Fang et al.'s works on flip-chip design [6], [7], [8] and Yu et al.'s work on package routing [9]. Note
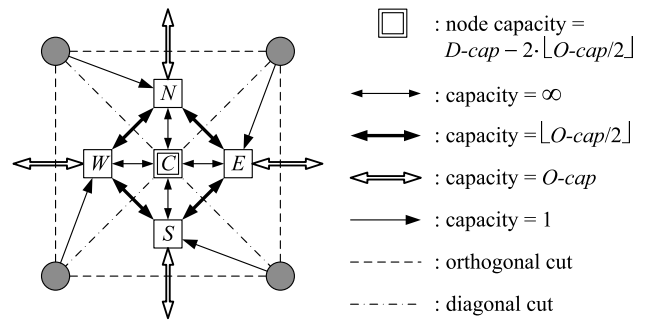
that Yu et al.'s work is not completely based on the network model in Fig. 2. Their network is based on triangulation of the pins because they do not assume a regular rectangular grid structure of the pins. In Wang et al.'s work on layer minimization [10], network-flow is used to analyze the problem and estimate the maximum number of escapable pins.

The model in Fig. 2 works well if we only consider orthogonal wiring capacity, which is the maximum number of wires allowed between two horizontally or vertically adjacent pins. It does not capture the diagonal capacity because the number of wires passing between two diagonally adjacent pins cannot be correctly captured by this model. Yan and Wong [11] proposed a network model that could correctly capture the diagonal capacity as well as orthogonal capacity. By adding nodes and edges, they are able to control the flow in finer detail inside each tile and thereby capture the diagonal capacity. Their network model is illustrated in **Fig. 3**. Their other contribution is to consider missing pins in their model.

There are also non-flow solutions to the unordered escape routing problem. For example, Yu and Dai [12], [13] used monotonic routing style to escape all the pins in a pin grid on one layer. However, non-flow solutions are usually used to solve full grid escape problem, which means all the pins in the grid are expected to be escaped in one or multiple layers, which is a common problem for package routing. In PCB routing, we often face the problem in which a set of specified pins is expected to be escaped on the same layer. In that case, network-flow is still the most popular approach.

3.2 Ordered Escape

For the ordered escape problem, network-flow does not work because flow does not carry the ordering information. Researchers usually rely on either heuristics that may lose optimality or exponential time approaches such as integer linear programming (ILP) or Boolean satisfiability (SAT).

In Ref. [14], Fang et al. formulated the ordered escape routing problem as an ILP problem and used an ILP solver to solve the problem optimally. With their reduction technique, they were able to prune the number of variables by 99.9%. Such a variable reduction is very useful because it reduces the runtime for a fairly large design (over 1,000 pins) to about an hour, which is acceptable considering human designers will spend much more time routing it manually. Unfortunately, since they consider nonmonotonic routing only when their routing graph has a cycle, their ILP formulation does not guarantee optimality.

In Ref. [15], Luo and Wong proposed to transform the ordered routing problem into a SAT problem and use a SAT solver. Their formulation makes no assumption on the routing style, meaning that their approach can guarantee to find a solution if one exists. It is the first work that can optimally solve the ordered escape routing problem. However, this optimality comes at a price. It would take the router about 10 minutes to route a 10×10 grid and the time complexity grows very fast when the grid size increases. However, they also proposed a partition technique to decompose a large problem into smaller problems, which could significantly reduce the runtime. In a later paper [16], Luo and Wong extended their router to handle cyclic ordering and pin clustering. Because their router is very powerful in solving small but difficult problems, they also propose to use their router to rip-up and reroute a small region where other heuristic-based routers fail to complete the routing.

Another route that researchers took to tackle the problem is to simplify the problem by adding constraints on the routing. The most popular constraint used is the monotonic routing constraint. The escape routing of a pin is called *monotonic* if it goes to the target pin grid boundary without turning back. Kubo and Takahashi's work [17], [18] on two layer escape routing and via assignment for packages adopts this monotonic routing style. In their work, they assume that the escape routing follows monotonic style and perturb the via assignment iteratively to search for suitable via assignment and escape routing. This approach was then enhanced by Tomioka and Takahashi [19] to achieve better routability.

In another paper by Tomioka and Takahashi [20], they studied the cases where pins are escaped through a corner of a pin grid or through the opposite two sides of a pin grid. They discovered the necessary and sufficient conditions for planar topological solutions to exist in those two cases. They also proposed a routing algorithm based on the discovered necessary and sufficient conditions.

The work by Lee et al. [21] does not put monotonic constraint on the routing. Their routing algorithm is based on computing the *weighted longest common subsequence* and *maximum planar subset of chords*. They compared their router with the ILP-based router in Ref. [14] and showed a 122x speedup.
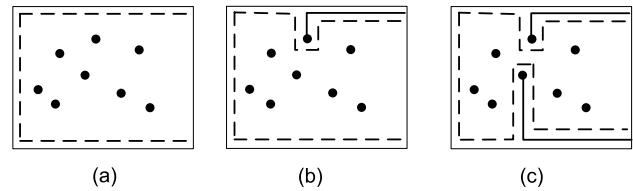

Fig. 4   An illustration of boundary routing [25].

3.3 Simultaneous Escape

Different from the single component escape routing problems which are common for both package and PCB routing, the simultaneous escape routing problem is unique to PCB routing. Therefore, there is less research in this category.

The earliest work on this problem is Ozdal and Wong's work [22], [23]. Their idea was to first generate a few simple routing patterns for each pin and then choose one routing pattern per pin such that the mismatched net ordering along the two boundaries is minimized. They intelligently modeled the pattern selection problem as a *longest path with forbidden pairs* problem and proposed an exact polynomial-time algorithm that is guaranteed to find the maximal planar routing solution on one layer. For large problems, they proposed a randomized algorithm that has better scalability. In a later paper [24], they presented several enhancements on this router: (1) they used a congestion-driven router to generate the routing patterns, and (2) they took performance constraints into consideration. The effectiveness of their approach is largely determined by the routing patterns generated in the first step. The router performs well when good routing solutions can be captured by the generated patterns. Unfortunately, the shape of the escape routing can be very complicated in difficult escape problems. In this case, it can be very tricky to predict what patterns should be generated to capture a good solution.

In Ref. [25], Luo et al. presented a novel *boundary routing* approach to solve the simultaneous escape routing problem. Essentially, their idea is to build a routing boundary for all the pins inside a pin grid and let the routing path follow the boundary as much as possible when routing a net. After a net is routed, the routing boundary is shrunk to exclude the routed net. **Figure 4** illustrates this idea. Although their strategy looks very simple, experiments show that this strategy is very effective in solving difficult problems. For a set of industrial escape problems, their router successfully solved all of them while the Cadence Allegro PCB router was only able to complete the routing for half of the problems. **Figure 5** shows their routing result for one problem.

One interesting work worth mentioning is the *potential router* proposed by Kajitani [26]. The idea is based on the analogy between planar routing and equipotential lines in an electric field. Equipotential lines are naturally planar. Therefore, we can view any planar routing as the equipotential lines in a certain electric field. On the other hand, by enumerating possible configurations of the electric field, one could enumerate possible planar topologies for the routing. Since this work focuses on planar topology in general, its theory can be applied to all three types of escape routing problems.
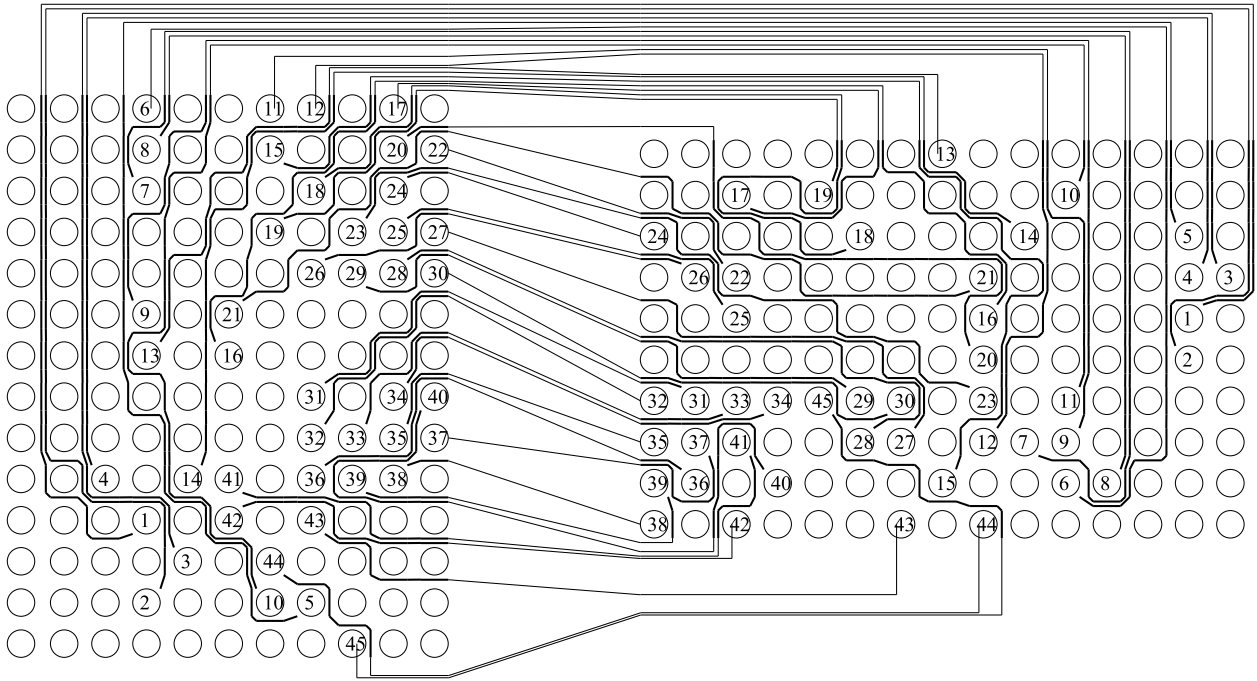
Fig. 5   Simultaneous escape routing solution produced by Luo et al.'s router [25].

4. Bus Escape Planning

Works in the previous section consider the escape routing problems at net level. On the other hand, Kong et al. started a series of works studying escape routing problems on bus level [27], [28], [29], [30], [31]. In these works, they adopt a *projection based* escape routing style. The escape routing of each bus is bounded by a rectangle formed by projecting the pin cluster of the bus toward the boundary of the pin grid (see **Fig. 6**). In Ref. [30], they compare their projection based pin assignment and escape routing solution with the single-layer escape routing solution and observe that the projection based multi-layer solution usually results in shorter wire length and occupies smaller routing space. **Figure 7** illustrates this argument. It can be seen that the multi-layer routing solution produced by their projection based scheme has shorter and straighter wires. Moreover, if we escape all the pins in one layer, we will obtain very imbalanced wire length: some pins have very long detours in their escape routing while some other pins escape without any detour. This dramatic difference in wire lengths makes later length-matching routing a much more challenging problem. On the other hand, the projection based multi-layer solution has very straight wires. Therefore, the length difference is much smaller, making length-matching routing an easier problem.

The bus escape planning problem is to plan the routing area for each bus so that there are no conflicts between the buses. Under the projection based escape routing framework, the routing area of a bus is its projection rectangle. Therefore, the bus escape planning problem can be abstracted as a rectangle arrangement problem: assign the given projection rectangles to the routing layers so that the following two conditions are satisfied on each layer:

- **Non-overlap constraint:** The projection rectangles inside a pin array do not have any overlaps. Otherwise, the escape
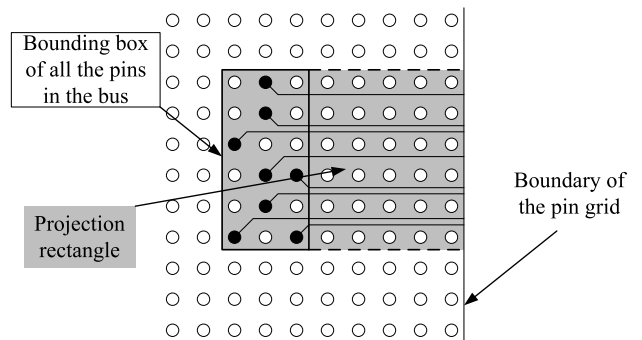

Fig. 6   Projection based escape routing style.

routing inside the two rectangles can potentially overlap (see **Fig. 8** (a)).
- **Planar constraint:** The ordering of the projection rectangles along the boundaries of the two pin arrays must match (similar to simultaneous escape routing problem). Otherwise, the two buses will cross each other (see Fig. 8 (b)).

Notice that all the projection rectangles have one property: at least one edge of the projection rectangle must be attached to the pin array boundary.

Similar to the escape routing problem, the bus escape planning problem also has different flavors:
- **Escape planning** considers one pin array (as shown in **Fig. 9** (a)). There is no planar constraint in this case, and only the non-overlap constraint needs to be considered.
- **Simultaneous escape planning** considers two pin arrays (as shown in Fig. 9 (b)). Both the non-overlapping and the ordering constraints must be satisfied on each layer.

We will survey the works under the two categories in the subsequent subsections.
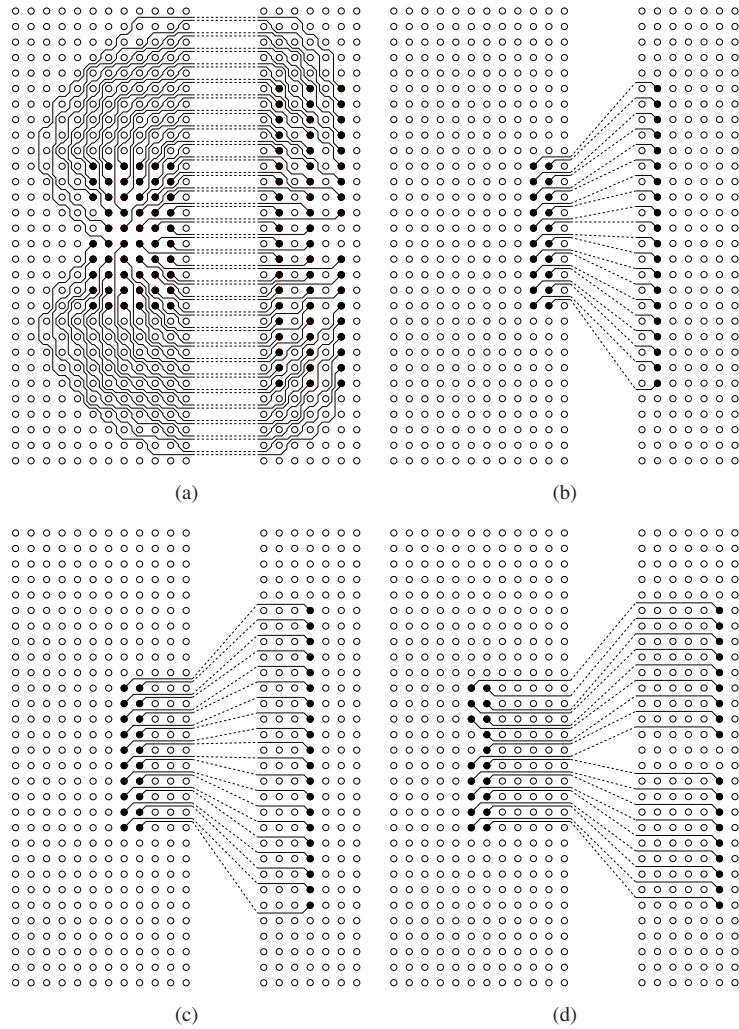
Fig. 7 Single-layer escape vs. projection based multi-layer escape. (a): single-layer escape routing; (b),
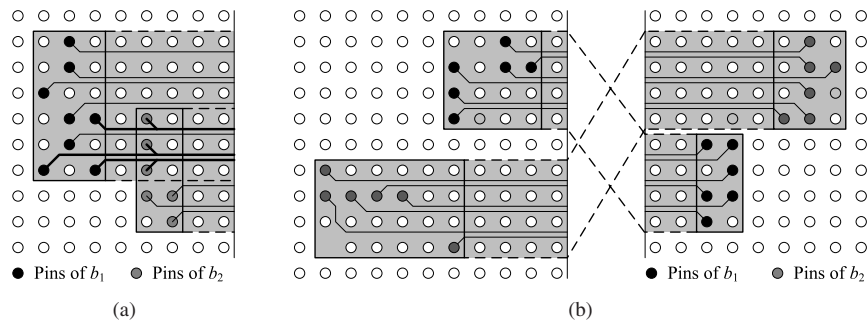(c), (d): projection based 3-layer escape routing.

Fig. 8 Conflict between projection rectangles. (a): overlapping rectangles in a pin array lead to over-
lapping escape routing; (b): reversed ordering of the rectangles in two pin arrays leads to wire
crossing of two buses.

4.1 Escape Planning

Kong et al. first studied the escape planning problem in
Ref. [29], in which they proposed an optimal algorithm to find a
maximum non-overlapping subset of the projection rectangles. In
their approach, the simpler cases are first solved by dynamic pro-
gramming, where the projection rectangles are attached to one or
two sides of the pin array; the more complicated cases where the
projection rectangles are attached to three or four sides are then
solved by an enumeration technique and reduction to the simpler
cases. The time complexity of their algorithm is $O(n^6)$, where

n is the number of input projection rectangles. Note that each
bus has four possible projection rectangles to the four sides of the
pin array. The four rectangles overlap at the pin cluster bound-
ing box. If all four projection rectangles of a bus are fed to the
input, the algorithm can choose at most one of them. Therefore,
by feeding all four possible projection rectangles of each bus to
the algorithm, the optimal escape directions of the buses can be
automatically determined. In a subsequent work [31], Ma et al.
studied the problem of determining the optimal projection direc-
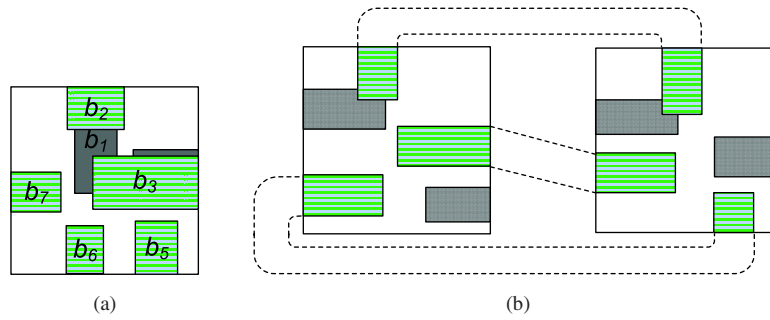tions of the buses such that the resultant maximum clique size of

Fig. 9 Two types of bus escape planning problem. (a): escape planning; (b): simultaneous escape planning. The striped rectangles in each figure form a selected subset without conflict.

the projection rectangles, i.e., the maximum number of projection rectangles overlapping with each other, is minimized. It is easy to see that the maximum clique size of the projection rectangles is a lower bound of the number of layers needed. Suppose the maximum clique size is k (each pair of the k projection rectangles overlap), at least k layers are required to accommodate all the buses. The maximum clique size is usually a good estimate of the minimum number of layers needed. The authors prove that this problem is NP-complete by reduction to the 3SAT problem. They then provide a good approximation algorithm to solve it using linear programming relaxation and rounding.

4.2 Simultaneous Escape Planning

Simultaneous escape planning is first studied in Refs. [27], [28]. In these two works, they consider the case where the two pin arrays are placed "face to face" and the projection rectangles in both arrays are all attached to the two facing boundaries. In Ref. [27], Kong et al. tackled the problem of selecting a maximum subset of projection rectangles satisfying both the non-overlap and planar constraints. Since all the projection rectangles are attached to the two facing boundaries, each projection rectangle can be viewed as an interval along the facing boundaries. The problem is then transformed into a longest common interval sequence (LCIS) problem and solved optimally by dynamic programming in $O(n \log n)$ time, where n is the number of projection rectangles. Yan et al. [28] then studied the layer assignment problem, which is to assign the projection rectangles into a minimum number of layers without conflict. They show that the layer assignment problem can be transformed into a bipartite matching problem, which can be optimally solved in $O(n^{2.38})$ time. By finding the maximum matching of the corresponding bipartite graph, the optimal layer assignment of the projection rectangles can be easily obtained.

In a recent work [32], Ma et al. studied the layer assignment problem of the general case simultaneous escape planning, where the projection rectangles can be attached to any boundary of the pin arrays. An optimal algorithm based on branch and bound search is proposed to assign the projection rectangles into a minimum number of layers, such that the non-overlap and planar constraints are satisfied on each layer. The search process starts from the root of the search tree and visits different parts of the tree by assigning certain projection rectangles to specific layers. At each tree node, a lower bound and an upper bound are computed using

ILP, and the subtree is pruned if it does not lead to an optimal solution. A min-cut based ordering algorithm is also developed to preprocess the projection rectangles, so that the projection rectangles in the search tree are properly ordered, which makes early pruning more possible and further improves the searching efficiency. Experimental results report reasonable runtime.

5. Length-Matching Routing

Length-matching routing is to connect the escaped routes between the boundaries of pin arrays while satisfying certain length constraints. Due to the high clock frequencies on today's high-performance boards, the nets are usually subject to very stringent length constraints. There are two types of length-matching constraints:

- **Min-max length bounds**: Each net is given minimum and maximum length bounds and the length of the routing must be within the bounds.
- **Bounded length difference**: A group of nets are expected to have similar length. In other words, the difference between the lengths of a group of nets must be limited by some given bound.

In order to meet the minimum length bound or to minimize the length difference, we may need to lengthen wires that are too short. This makes the length-matching problem unique because intentionally increasing the wire length is usually discouraged in many other routing problems.

A common way to increase the wire length is to snake the wire. However, snaking one wire generates a large blockage for other wires. In order to avoid this blockage, other wires may need to be detoured, potentially causing their maximum length bounds to be violated. As a result, greedy approaches will usually fail because they lack the global view of balancing the needs of all the wires. How to carefully distribute the limited routing resources so that the length requirements of all the nets can be satisfied is the key to this problem.

The first work that does non-greedy resource allocation for wire extension is by Ozdal and Wong [33], [34]. They used a Lagrangian relaxation based routing scheme to control the length of each net. In their routing scheme, Lagrangian multipliers are iteratively updated to reflect the current resource need of each net. A special router is called in each iteration to route the nets according to the resource need implied by the multiplier. In general, their approach provides good results. However, it has two
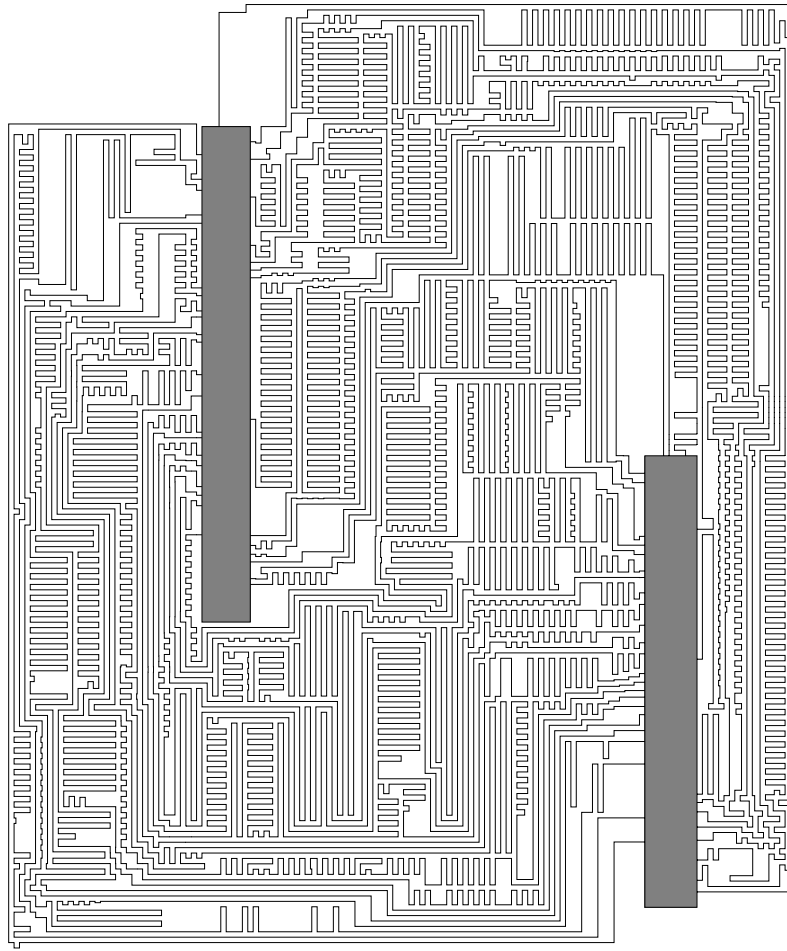
Fig. 10   The routing result of Yan and Wong's [38] length-matching router.

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potential issues:

- A router must be called *iteratively* to perform the actual routing. When the problem is large and difficult, it needs many iterations to converge to a solution, resulting in very long runtime.
- The routing of each net must be monotonic in one direction. This limits the possible topology of the solution and therefore also the application of this approach.

In a later work, Ozdal and Wong [35], [36] proposed an algorithm for length-matching routing inside a channel. They first used river routing to derive the routing boundary of each net and then detoured each net inside its bounded area. They showed that their algorithm can approximate the optimal solution by a constant factor. This approach can achieve quite significant speedup compared to the Lagrangian relaxation based approach because it avoids calling a router iteratively. However, since only the channel routing problem is considered, this approach has even more limited applications.

Length-matching routing inside a channel is also challenged by Kubo et al. [37]. They used a *symmetric-slant grid interconnect* scheme to reduce the length-matching problem into a general grid routing problem. The advantage of their work is that it can also handle multi-sink nets. However, their approach is for IC routing and therefore assumes an XY routing style, which is not practical

for PCB routing.

Recently, Yan and Wong [38] proposed a length-matching algorithm that does not impose any restriction on the routing topology. Neither does their router require the pins to be aligned along a channel, nor does it limit the routing to be monotonic. Their key idea was to view the length-matching routing problem as an area assignment problem and use a placement structure, bounded-sliceline grid (BSG) [39] to help transform the area assignment problem into a mathematical programming problem. An iterative approach was then used to solve this mathematical programming problem. Besides its ability to handle general topology, another big advantage of this router is that it is gridless. Unlike all previous routers, its performance does not depend on the routing grid size. This feature leads to very good scalability and is extremely useful because modern PCB routing configurations usually imply huge routing grids. This advantage was verified by their experiments. In one of their data, they achieved a 1000x speedup over the Lagrangian relaxation based router in Ref. [34]. Their router is very effective in solving difficult problems. **Figure 10** illustrates one of their routing results. It can be seen that their router could efficiently utilize the routing space for wire extension. In a later paper [40], they extended their router to handle multi-layer routing and multiple separation rules.

One potential drawback of their work is that their routing

scheme assumes a given topology. Such a topology is easy to generate if there are not many obstacles. However, if the design is filled with many obstacles, then generating a good topology for their router could be non-trivial. Two different solutions were recently proposed to address this issue:

Yan and Chen [41] follow the overall framework of first partitioning the routing area into regions and then assigning routing resources in the regions into individual nets proposed in Refs. [38], [40]. However, their ways of partitioning the routing area, generating routing topology and assigning routing resources are more sophisticated. Instead of using a sizable structure (BSG), they generate the partition by merging neighboring regions in the Hanan grid. The routing topology is then determined by applying the max-flow algorithm on the adjacent graph generated from the partition. Finally, the routing resources in the regions are utilized to detour/straighten the nets to meet the length constraint through a sequence of heuristics. The experimental results show the great potential of their router.

Kohira and Takahashi [42], [43] took a completely different approach. Their idea is to expand the wavefront of all the nets simultaneously. When expanding the wavefront of one net, the router tests the connectivity of all nets via max-flow algorithm and determines the feasible directions of wavefront expansion. Then it greedily chooses from the feasible directions the one that minimizes the difference between the current estimated length and the given length constraint. The result is promising in the presence of many obstacles. Since the max-flow algorithm is used to test connectivity on each wavefront expansion, this approach guarantees that all pins will eventually be connected. However, since the algorithm is greedy and lacks a global prospect of resource allocation, the router can make wrong choices during the course of wavefront expansion. As a result, the length error of their approach is fairly large. To address this issue, they proposed some post-process operations such as R-Flip and S-Flip to heuristically detour/straighten the wires in order to reduce the length error.

6. Other Works

There are many other works on PCB layout that do not fall into the previous categories.

Yan and Wong [44], [45] proposed a preprocessing step to untangle the twisted nets for length-matching routing. They proposed a single-detour routing style and did a series of theoretical studies on this style. Their work was then followed up by Yan and Chen [46], who considered untangling on both ends of the routing.

Global planning of buses is studied by Kong et al. in Ref. [47]. They proposed the first automatic bus planner for PCB routing. Their bus planner not only performs global routing of buses on each layer, but also does layer assignment. They tested their planner on a state-of-the-art industrial board (7000+ nets and 12 layers) and achieved very good routability. Length constraints were also considered in their work.

The pin assignment problem for PCBs is studied in Ref. [48]. In the paper, Meister et al. proposed four heuristics for pin assignment considering both wire length and routability; however, they did not perform escape routing. A simultaneous pin assignment

and escape routing scheme is proposed in Ref. [30].

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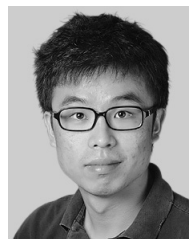
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