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# Decoders for Double-Length SbEC-DbED Codes

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With the advent of high-density semiconductor chips, $b$-bit organized RAM chips have been fabricated and are now being marketed. Such memory systems use single $b$-bit byte error correcting and double $b$-bit byte error detecting codes (SbEC-DbED codes) to increase the reliability. This paper describes some new decoders for SbEC-DbED Reed-Solomon codes, with a data length of $k = 128$ bits and a byte length of $b = 4$ bits. Since these codes are based on Reed-Solomon codes, the decoders are constructed by using the regulality of the parity-matrix of Reed-Solomon codes and they have about 18 percent less gate circurity than conventional decoders.

## 1. Introduction

The bit length of a computer's main memory is typically 64-bits in a general-purpose computer or 32-bits in a work station. However, these bit lengths are often increased to 128-bits, especially for cache memory. The error-correcting codes currently used are SEC-DED-D4ED codes[2]and S4EC-D4ED codes[1),2)]. Both have advantages and disadvantages. The latter are considered to be efficient when a RAM for 4-bit organized processing is used. In this paper, we propose new SbEC-DbED (single $b$-bit byte error correcting and double $b$-bit byte error detecting) codes, with a byte length of $b = 4$ and a data length of $k = 128$, for a high-speed decoder.

## 2. Some New Double-Length SbEC-DbED Codes

$T$ is a companion matrix; for example, the companion matrix of GF($2^4$) is defined by $g(X) = x^4 + x + 1$ as

$$T = \begin{pmatrix} 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{pmatrix} \qquad (1)$$

Here, the elements of GF($2^b$) can all be expressed by $i$th power of $T$. $T$ is essentially the same as the regularly used $\alpha$.

First, we show the fundamental form of the parity-check matrix Reed-Solomon single $b$-bit byte error correcting and double $b$-bit byte error detecting codes (hereafter abbreviated as R-S SbEC-DbED codes) with a minimum distance of 4.

$$H = \begin{pmatrix} 1 & 1 & \cdots 1 \cdots & 11100 \\ T^{(q-2)} & T^{(q-3)} & \ldots T^i \ldots & T1010 \\ T^{2(q-2)} & T^{2(q-3)} & \ldots T^{2i} \ldots & T1010 \end{pmatrix} \qquad (2)$$

where, $q = 2^b$. The maximum code length for the R-S SbEC-DbED codes is $n = b \cdot (2^b + 2)$. Hence, R-S SbEC-DbED codes, which have $k = 64$-bit and, 128-bit data length, cannot be constructed for byte lengths of $b = 2, 3$ and 4 bits.

Assuming that the syndrome of codes using Eq. (2) is $S = (S_0, S_1, S_2)$, the error location number is $x_1 = T^i$, and the error value is $Y_1$, then the syndrome of a single-byte error is $(S_0 = Y_1, S_1 = Y_1 x_1 = Y_1 T^i, S_2 = Y_1 T^{2i})$. Accordingly, the error location number is $x_1 = T^i = S_1/S_0 (= S_2/S_1)$ and the error value is $Y_1 = S_0$.

Basically, in order to estimate the number of error digits, we can use

$$M_f = \begin{pmatrix} S_l & S_{l+1} & \cdots & S_{l+f-1} \\ S_{l+1} & S_{l+2} & \cdots & S_{l+f} \\ \cdots & \cdots & \cdots & \cdots \\ S_{l+f-1} & S_{l+f} & \cdots & S_{l+2f-2} \end{pmatrix} \qquad (3)$$

If $f$ errors occur, $M_f \neq 0$, and if fewer than $f$ errors occur, $M_f = 0$[3)].

By substituting $l = 0$ and $f = 2$ into Eq. (3), we can obtain an error-discriminating equation $Z$ for R-S SbEC-DbED codes as

$$Z = S_0 S_2 + S_1{}^2 \qquad (4)$$

Then, we can judge that a single-byte error occurs if $Z = 0$ and that double-byte errors occur if $Z \neq 0$.

However, this method has never been used in order to judge errors in R-S SbEC-DbED codes. The errors treated in Eq. (3) can be corrected, whereas only two errors, in this paper, can only

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be detected, but not corrected.

The following equation equivalent to Eq. (4) can also be used as an error discriminating equation in R-S SbEC-DbED codes.

$$Z = (S_0T^i = S_1 \text{ AND } S_1T^i = S_2) \quad (5)$$

Namely, at each byte point $T^i$, we check Eq. (5), and a single-byte error is detected at the byte point whose error-byte-pointer is 1, namely where $Z$ is true. Moreover, double-byte errors are detected when the syndrome is nonzero and none of the error byte pointers indicates an error.

Here, the error in the check byte, for example at $(100)^t$, is detected when $S_0 \neq 0$(namely, $S_0$ is an error pattern), $S_1 = 0$ and $S_2 = 0$.

**Theorem 1** Let $H_0$ be the $H$ matrix of an $(N, N-R)$ SbEC-DbED code, where $N = n \cdot b$, $R = r \cdot b$ [1),2)]. The code defined by the following $H$ matrix is a $(2N, 2N-R-b)$ SbEC-DbED code.

$$H = \begin{pmatrix} H_0 & H_0 \\ 0\,0\,0 \cdots 0 & 1\,1\,1 \cdots 1 \end{pmatrix} \quad (6)$$

Using Theorem 1, we derive a new parity-check matrix of the double-length R-S SbEC-DbED codes. First, we locate the first matrix inserted $(11 \cdots 1)$ above the parity-check matrix (2) and then we locate the second matrix inserted $(00 \cdots 0)$ above the parity-check matrix (2) next to the first matrix. The codes with this linked matrix have minimum distance 4; that is, they are SbEC-DbED codes.

Next, we add the first row to the second row in the linked matrix. Then, we obtain a $(4 \times 4)$ identity matrix as a parity-check matrix by transposing $(1000)^t$ from the center of the matrix to the fourth column from the right. By further transposing the two rows of $(1110)^t$ and $(1101)^t$ from the center to the left column of the identity matrix, we derive the matrix (7).

As Eq. (7) has been obtained from Theorem 1 and elementary row operation[4)], it is evident that the codes with Eq. (7) have distance 4. Therefore, Eq. (7) is a parity-check matrix of double-length R-S SbEC-DbED codes.

Next, we obtain a new parity-check matrix of 2-modularized double-length SbEC-DbED codes. The parity-check matrix of 2-modularized SbEC-DbED codes (Eq. 8) is obtained from Eq. (2) by a linear operation.

Modules (a) and (b) shown in Eq. (8) have the same three row vectors. The usual parity-check matrix 2-modularized SbEC-DbED codes is obtained by getting rid of $(111)^t$ from Eq. (8) [1),2)]. The product of the second row and the third row can be made to be a certain value $T^c$. In this case, $(1\ T^{c/2}\ T^{c/2})^t$ is transposed in front of the $(3 \times 3)$ identity matrix.

$$H = \left(\begin{array}{cccc|cccc|cc|cccc} 1 & 1 & \cdots\cdots & 1 & 0 & 0 & \cdots\cdots & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & \cdots\cdots & 0 & 1 & 1 & \cdots\cdots & 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ T^{q-2} & T^{q-3} & \cdots\ T & 1 & T^{q-2} & T^{q-3} & \cdots\ T & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ T^{2(q-2)} & T^{2(q-3)} & \cdots\ T^2 & 1 & T^{2(q-2)} & T^{2(q-3)} & \cdots\ T^2 & 1 & 0 & 1 & 0 & 0 & 0 & 1 \\ & & & & & & & & K_1 & K_2 & C_1 & C_2 & C_3 & C_4 \end{array}\right) \quad (7)$$

A-block B-block K-block C-block

$$H = \begin{pmatrix} 1 & \cdots & 1 & 1 & 1 & \cdots & 1 & 1 & 1\,1\,0\,0 \\ T^p & \cdots & T^2 & T^1 & T^{-p} & \cdots & T^{-2} & T^{-1} & 1\,0\,1\,0 \\ T^{-p} & \cdots & T^{-2} & T^{-1} & T^p & \cdots & T^2 & T^1 & 1\,0\,0\,1 \end{pmatrix} \quad (8)$$

module a module b

$$H = \begin{pmatrix} 1 & \cdots & 1 & 1 & \cdots & 1 & 1 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & 1 & 1 & 1\,0\,0\,0 \\ 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & 1 & \cdots & 1 & 1 & \cdots & 1 & 1 & 1 & 1 & 0\,1\,0\,0 \\ T^p & \cdots & T^1 & T^{-p} & \cdots & T^{-1} & 1 & T^p & \cdots & T^1 & T^{-p} & \cdots & T^{-1} & 1 & 0 & 1 & 0\,0\,1\,0 \\ T^{-p} & \cdots & T^{-1} & T^p & \cdots & T^1 & 1 & T^{-p} & \cdots & T^{-1} & T^p & \cdots & T^1 & 1 & 1 & 0 & 0\,0\,0\,1 \\ & & & & & & & & & & & & & & K_1 & K_2 & C_1\,C_2\,C_3\,C_4 \end{pmatrix} \quad (9)$$

A-block B-block K-block C-block

$$H = \begin{pmatrix} 1 & \cdots & 1 & 1 & \cdots & 1 & 0 & \cdots & 0 & 0\,1\,1\,1 & 1\,0\,0\,0 \\ 0 & \cdots & 0 & 0 & \cdots & 0 & 1 & \cdots & 1 & 1\,0\,1\,1 & 0\,1\,0\,0 \\ T^7 & \cdots & T^1 & T^8 & \cdots & T^{14} & & & & 1\,1\,0\,1 & 0\,0\,1\,0 \\ T^8 & \cdots & T^{14} & T^7 & \cdots & T^1 & (a & & b) & 1\,1\,1\,0 & 0\,0\,0\,1 \end{pmatrix} \quad (10)$$

A B K C

Here, we locate the first matrix inserted $(111\cdots1)$ above Eq. (8) and locate the second matrix inserted $(000\cdots0)$ above Eq. (8) next to the first matrix, and add the first row to the second row in the linked matrix. By transposing $(1000)^t$ from the center of the matrix to the fourth column from the right, we obtain a unit matrix, and by further transposing $(1110)^t$ and $(1101)^t$ to the leftmost side column of the unit matrix, we finally derive the matrix (9).

Here, substituting $b = 4$, $p = 2^b - 1 = 15$, $T^{15} = 1$ into Eq. (9), we derive the matrix (10) by transposing $(1011)^t$ and $(0111)^t$ to a block $K$, where (a b) is the same as the modules in Eq. (8).

The matrices (7), (9), and (10) are all parity-check matrices of double-length SbEC-DbED codes, and the minimum distance $d = 4$. Further, when one byte is $b$-bit, the code length is to be $n = (2^b + 2) \cdot b \cdot 2$ bits. Consequently, if $b = 4$, (144, 128) codes are composed, where code bit length $n = 144$, data bit length $k = 128$, and check bit length $c = 16$.

Here, the equations corresponding to Eqs. (4) and (5) applied to Eq. (8) are as follows:

$$Z = {S_0}^2 + S_1 S_2, \tag{11}$$

$$Z = (S_1 = T^i S_0 \text{ AND } S_2 = T^{-i} S_0), \tag{12}$$

where $(-p \le i \le p)$.

## 3. Some New Decoders for Double-Length SbEC-DbED Codes

First, we give a method for decoding the codes, using Eq. (7). We classify the code digits (or bytes) into blocks $A, B, K$, and $C$, as indicated below Eq. (7). Then, by using the syndromes $(C1, C2, C3, C4)$, we obtain

$$S_0 = C1 + C2, S_1 = C3, S_2 = C4. \tag{13}$$

Here, the syndrome $(S_0, S_1, S_2)$ can be treated in the same way as the syndrome for the R-S SbEC-DbED codes using Eq. (2), in blocks $A$ and $B$, respectively. Therefore, the decoding steps are as follows:

(1) If $C1 = C2 = C3 = C4 = 0$, we consider that no errors exist.

(2) We detect and correct a single error in block $K$, for example, by using a method that corrects the $K_1$ byte by the error value $C1$ if $C1 = C2 = C3 \neq 0$ and $C4 = 0$. The error value can be effectively obtained by calculating $C1 + C2 + C3 + C4$.

(3) We detect and correct a single error in block $C$, for example, by using a method that corrects the $C_1$ byte by the error value $C1$ if $C1 \neq 0$ and $C2 = C3 = C4 = 0$.

(4) We detect double errors in blocks $A$ and $B$, in $C_1$ and $C_2$, in $K_1$ and $C_3$, and in $K_2$ and $C_4$ if ($C1 \neq 0$ AND $C2 \neq 0$).

(5) By using $Z = {S_1}^2 + S_0 S_2 \neq 0$, we detect all of the double errors except the errors detected in step 4.

(6) If double errors are not detected in steps 4 and 5, we consider that a single error exists in block $A$ or $B$. Moreover, we consider that a single error exists in block $A$ if $C1 \neq 0$ ($C2 = 0$) and that a single error exists in the block $B$ if $C2 \neq 0$ ($C1 = 0$). The single error is corrected by using the error location number $X_1 = S_1/S_0$ and the error value $Y_1 = S_0$.

Next, we describe double-byte errors detection. Step 4 is clear, since the single error of block $K$ having ($C1 \neq 0$ AND $C2 \neq 0$) was corrected in step 2. The double errors in $K_1$ and $C_4$, and in $K_2$ and $C_3$ are also detected by ($C1 \neq 0$ AND $C2 \neq 0$). But all the double errors except those detected in step 4 can be detected by $Z = {S_1}^2 + S_0 S_2 \neq 0$, including these double errors. Details are given below. Here, the error values are $T^i$ and $T^j$, and the error location number in block $A$ or $B$ is $T^s$.

**(a)** Within the same block.

- Double errors in block $A$ or $B$ are detected by Eq. (4).
- Within block $C$.
  $C_1$ and $C_2$:: ($C1 \neq 0$ AND $C2 \neq 0$)
  $C_1$ and $C_3$:: $C1 = T^i$, $C2 = 0$, $C3 = S_1 = T^j$, $C4 = S_2 = 0$, $S_0 = C1 + C2 = T^i$, $Z = S_0 S_2 + {S_1}^2 = T^i \cdot 0 + T^{2j} = T^{2j} \neq 0$
  $Z$ can also be used for $C_1$ and $C_4$, $C_2$ and $C_3$, $C_2$ and $C_4$, or $C_3$ and $C_4$.
- Within block $K$.
  $K_1$ and $K_2$:: $C1 = T^i + T^j$, $C2 = T^i + T^j$, $C3 = T^i$, $C4 = T^j$, $Z = 0 \cdot T^j + T^{2i} = T^{2i} \neq 0$

**(b)** Between two blocks.

- Between blocks $A$ and $B$. $\cdots$ ($C1 \neq 0$ AND $C2 \neq 0$)
- Between blocks $C$ and $A$. (Since block $B$ is the same as block $A$, the explanation is omitted. )
  $A$ and $C_1$:: $C1 = T^i + T^j$, $C2 = 0$,

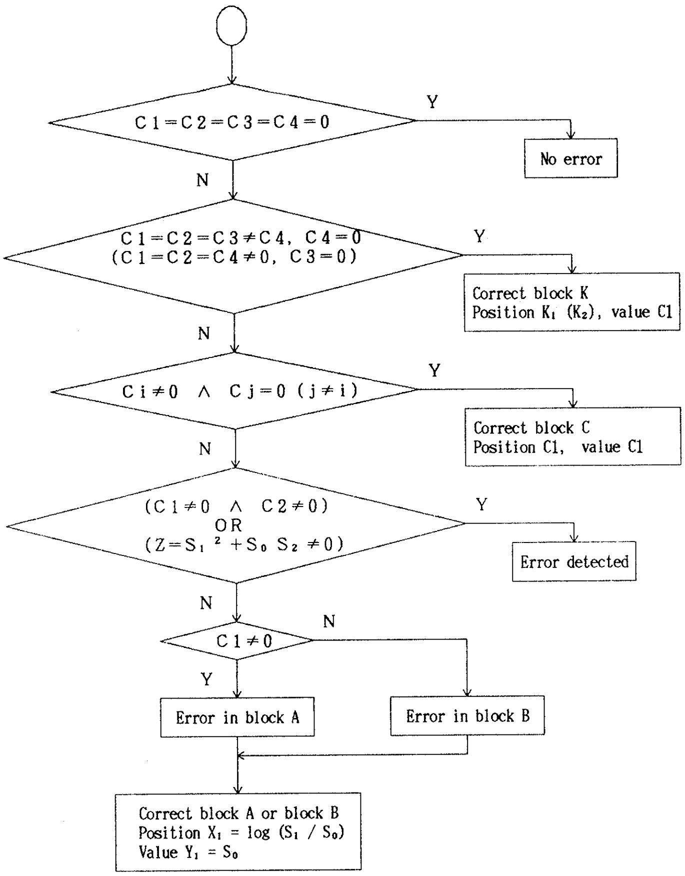


**Fig. 1** Flow chart for decoding double-length R-S SbEC-DbED codes.

$C3 = T^iT^s$, $C4 = T^iT^{2s}$,
$Z = (T^i + T^j)T^iT^{2s} + T^{2i2s}$
$= T^{i+j+2s} \neq 0$
Z can also be used for $A$ and $C_2$, $A$ and $C_3$, or $A$ and $C_4$.

- Between blocks $K$ and $A$. (Since block $B$ is the same as block $A$, the explanation is omitted.)
  $A$ and $K_1$:: $C1 = T^i + T^j$, $C2 = T^j$, $C3 = T^iT^s + T^j$, $C4 = T^iT^{2s}$,
  $Z = T^i \cdot T^iT^{2s} + (T^iT^s + T^j)^2 = T^{2j} \neq 0$
  $Z$ can be used for $A$ and $K_2$.
- Between blocks $K$ and $C$.
  $K_1$ and $C_1$:: $C1 = T^i + T^j$, $C2 = T^i$, $C3 = T^i$, $C4 = 0$,
  $Z = T^j \cdot 0 + T^{2i} = T^{2i} \neq 0$
  $K_1$ and $C_3$:: $(C1 \neq 0$ AND $C2 \neq 0)$
  $K_2$ and $C_4$:: $(C1 \neq 0$ AND $C2 \neq 0)$
  $Z$ can be used, for $K_1$ and $C_2$, $K_1$ and $C_4$, $K_2$ and $C_1$, $K_2$ and $C_2$, or $K_2$ and $C_3$.

As explained above, all double-byte errors can be detected by detecting that $ZZ = (C1 \neq 0$ AND $C2 \neq 0)$ $OR$ $(Z = {S_1}^2 + S_0S_2 \neq 0)$ is true.

**Figure 1** shows a decoding flow chart for double-length R-S SbEC-DbED codes.

**Figure 2** shows a decoder for double length R-S Sbec-DbED codes. Here, the vector expression and the exponent expression are used to express the elements of the Galois fields. Depending on the condition, whichever is more effective should be employed. The solid line indicates that the bit length is $b$ and the dotted line indicates that the bit length is 1. The symbol "+" represents exclusive OR-circuit, "ROM VE" is a ROM for transforming the element of the vector expression into an exponent expression, and the error-point-detection circuit using pattern coincidence (EPDC-PC) detects, for example,

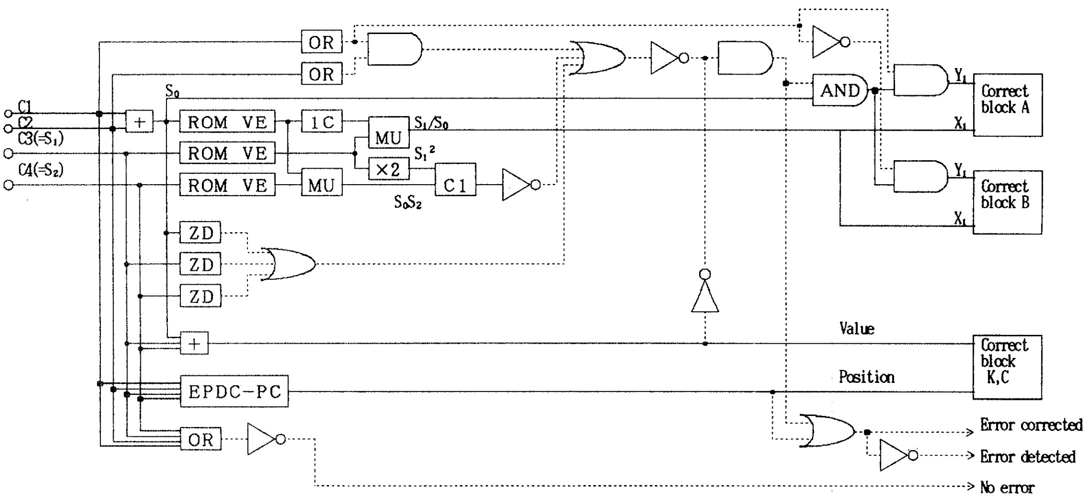


**Fig. 2** Decoder for double-length R-S SbEC-DbED codes.

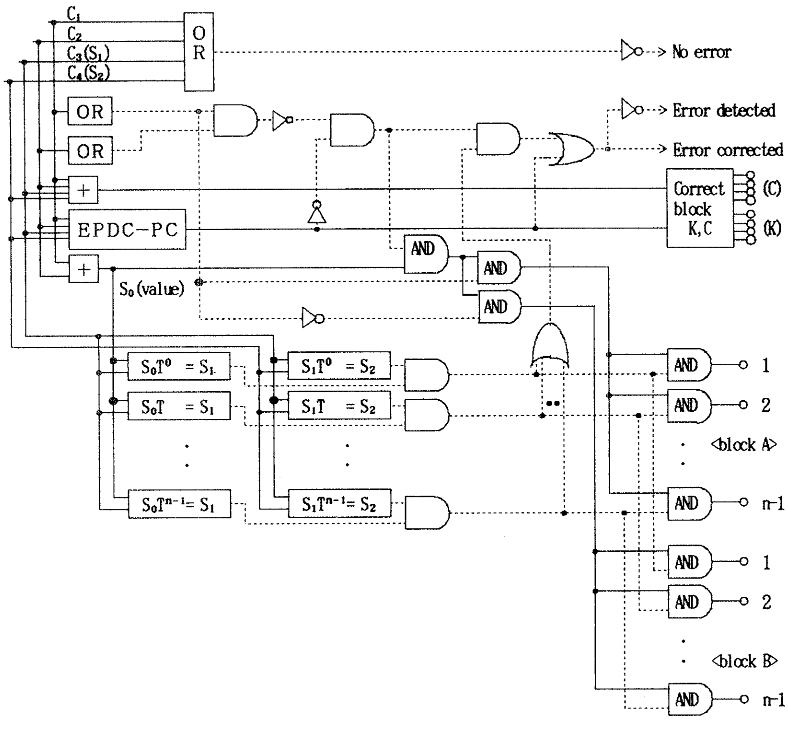


**Fig. 3** High-speed decoder for double-length R-S SbEC-DbED codes.

an error in the $K_1$ byte if $C1 = C2 = C3 \neq 0$ and $C4 = 0$. MU is used to obtain the sum of the elements of the exponent expression. 1C is used to obtain 1's complement, and in combination with MU, to obtain the difference of the elements. CI is a coincidence-detection circuit, and ZD is an all-$b$-bit zero-detection circuit.

Here, a no-error signal is output if $C1 = C2 = C3 = C4 = 0$. For errors in blocks $K$ and $C$, we obtain the error point by means of the error-point-detection circuit using pattern coincidence (EPDC-PC), and then obtain the error value by calculating $C1 + C2 + C3 + C4$ and correct the error. The syndrome ($S_0 = C1 + C2, S_1 = C3, S_2 = C4$) is then obtained. The output $S_1/S_0$ of MU gives the error location number $X_1$ of blocks $A$ or $B$, and the error value is $Y_1 = S_0$. If the error-identifying equa-

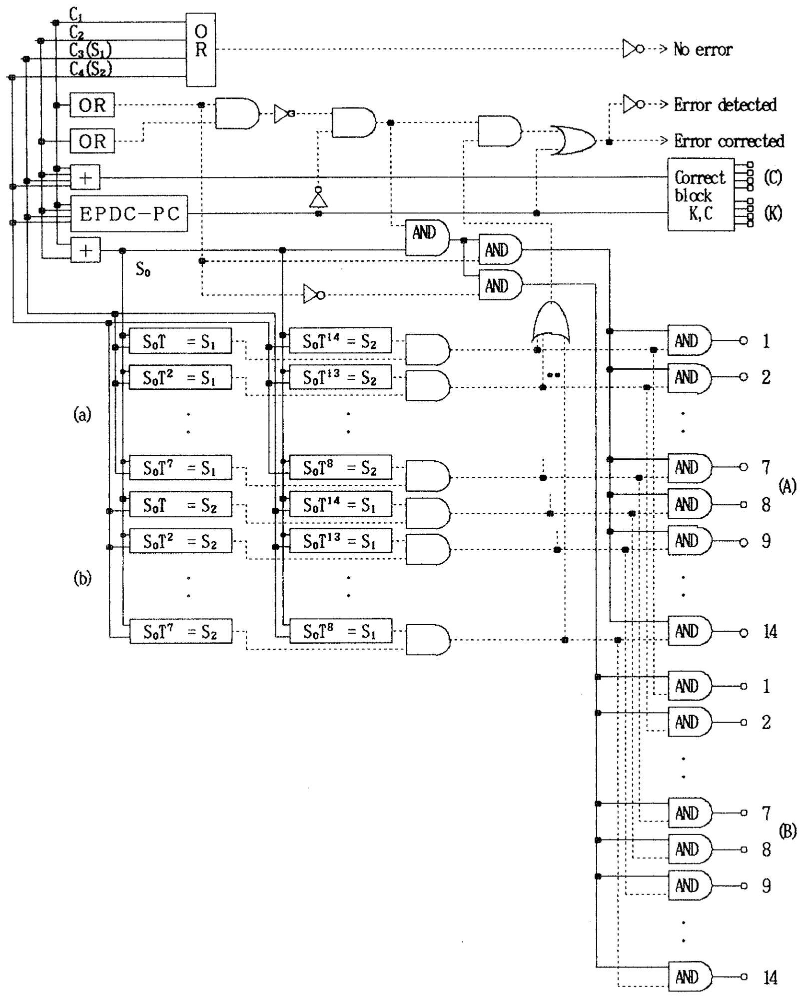


**Fig. 4** High-speed decoder for double-length SbEC-DbED codes (2-modularized codes).

tion is $Z = {S_1}^2 + S_0S_2 = 0$, the output of CI is 1. Three signals — the inverted signal, the signal of ($C1 \neq 0$ AND $C2 \neq 0$), and the signal that any one of $(S_0, S_1, S_2)$ is detected to be zero ($S_0$, $S_1$, and $S_2$ are not zero if there is a single error in the blocks $A$ or $B$) — are constructed as an OR signal and are made to be the error-detection signal. Then, the error-detection signal is inverted and used as a single error-correction signal in blocks $A$ and $B$, and carry out the operation only if no errors exist in blocks $K$ and $C$. Moreover, in correcting a single error in blocks $A$ or $B$, we correct the error in block $A$ if $C1$ is not zero, and correct the error in block $B$ if $C1$ is zero.

**Figure 3** shows a high-speed decoder for double-length R-S SbEC-DbED codes. In place of $Z = {S_1}^2 + S_0S_2 = 0$ in the decoder shown as Fig. 2, we use ($S_0T^i = S_1$ AND $S_1T^i = S_2$), in parallel, at each byte point $i$, and obtain the error byte pointer. The error value $S_0$ is sent to block $A$ if $C1 \neq 0$ and to block $B$ if $C1 = 0$, and the error of the point at which an error point signal is output is corrected.

This decoder is simple because it detects the positions of single errors in blocks $A$ and $B$ by means of the common circuit using the identifying equation $Z = {S_1}^2 + S_0S_2 = 0$ or ($S_0T^i = S_1$ AND $S_1T^i = S_2$). In Fig.3, the OR signal is generated from the signals of the error byte pointer, and double errors are detected when this OR signal is not output. In place of this method, we can get rid of the OR circuit and add a circuit detecting $Z = {S_1}^2 + S_0S_2 \neq 0$, in order to detect double errors. This simplifies circuit production and wiring, since the circuits for detecting ($S_0T^i = S_1$ AND $S_iT^i = S_2$) are equal.

**Figure 4** shows a 2-modular type decoder for double-length SbED-DbED codes. The parity-check matrix is (10). The decoder is the same as the one shown in Fig. 3, accordingly, when the syndrome is generated as ($S_0 = C1 + C2, S_1 = C3, S_2 = C4$), a single error in block $A$ or $B$ is detected by using the same identifying equation $Z = S_0{}^2 + S_1S_2 = 0$ or ($S_1 = S_0T^i$ AND $S_2 = S_0T^{-i}$), and all double-byte errors can be detected if $Z = (C1 \neq 0$ AND $C2 \neq 0)$ OR $(Z = S_0{}^2 + S_1S_2 \neq 0)$ is true (this can be proved in the same way as for the codes in Eq. (7)). Here, because of modules type, the error-byte-pointer-detection circuits for module blocks (a) and (b) are identical; The decoders in Figs. 3 and 4 have equivalent efficiency. The total number of gates is about 2660, calculated by the method in Ref. 1). The gate complexy is 82 percent less than that of the decoder described by Kaneda and Fujiwara[2], which uses the cyclic method, and the propagation delay is nearly equal.

## 4. More Double-Length Codes

We can construct more double-length codes, by using Theorem 1. For example, (256, 236) codes are obtained over (144, 128) codes. But circuits are almost the same as those for only one block, and therefore the gate complexity hardly increases.

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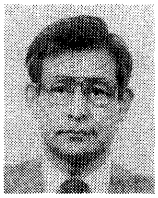

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