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A DESIGN OF A MULTIPROCESSOR SYSTEM USING MULTIPLE COPIED MEMORIES

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1. Introduction

In the past multiprocessor systems have been developed using multiple buses instead of a single bus as the network to reduce the contention for the bus. But contention also occurs for the common memories because more than one processors may want to access a common memory at the same time. If this happens, only one of them can get the permit of accessing and the others have to wait. This greatly degrades the system performance.

This paper proposes a multiple bus multiprocessor system with L-copied memories which permits simultaneous accesses to resolve the contention of common memory accesses. The performance of the proposed system is analyzed. Hence we have found that the performance of the proposed system is much more superior to that of previous single common memory systems.

2. The Model

The system consists of N processors and M L-copied memory modules connected by B global buses represented by N*(M-L)*B as shown in figure 1. Every processor is also connected to a private memory. Each memory module contains L identical memories and a duplicator . For simplicity we first deal with the case of two identical memories ie. L=2 which permits two reads and one write accesses simultaneously. The processor in the system works as follows :

At first it accesses the private memory for the program and local data and executes. From time to time it has to access the common memories both to write and to read. If there is a memory module conflict it has to wait until no more conflict exists. A memory module conflict happens when more than one processors want to write in or more than two processors want to read from the same memory module. If there is no memory module conflict but there is a memory location conflict the request is rejected and the processor has to request again in a random time. During this time it remains idle. Even though there is neither memory module conflict nor memory location conflict but if no bus is available, it has to wait until bus idle, otherwise it can access immediately. The time it needs for accessing is called access time. On finishing accessing it soon releases the bus and returns to active state ie. executing by using private memory and requests for access again in a random time.

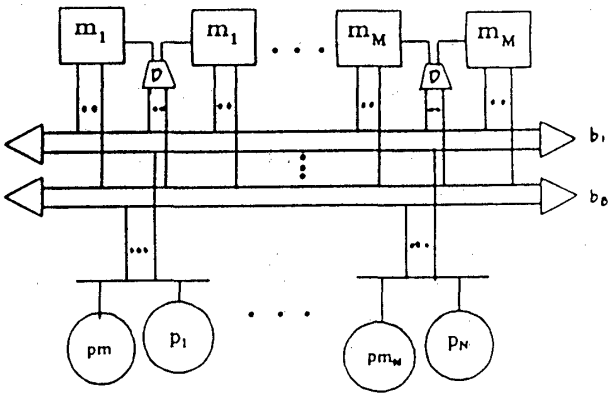

Figure 1

Assumptions

(a). The access time (both read and write) is exponentially distributed with the average $1/\mu$

(b). Each processor in active state requests for commom memory access in a exponentially distributed request rate with the average λ

(c). The rejected request due to memory location

conflict requests again in a exponentially distributed rate with the average λ

(d). When a processor requests access to common memory it requests for reading and writing in probabilities β and $(1-\beta)$ respectively

(e). The location conflict occurs in probability $(1-\alpha)$

(f). Any processor accesses all the memory modules uniformly ie. in the same probability 1/M

3. Performance Evaluation

We use processing power as the performance measurement. The processing power is defined as the average number of active processors.

A markov chain can be established if the system state is chosen as follows :

$$S=(n_{r_1}, n_{r_2}, n_{w_1}, n_{r_1w_1}, n_{r_2w_1}, n^{(1)}_{qw_1w}, n^{(1)}_{qr_2r}, n^{(1)}_{qr_1w_1w}, n^{(1)}_{qr_2w_1w}, n^{(1)}_{qr_2w_1r}, \ldots, n^{(B)}_{qw_1w}, n^{(B)}_{qr_2r}, n^{(B)}_{qr_1w_1w}, n^{(B)}_{qr_2w_1w}, n^{(B)}_{qr_2w_1r}, n^{(1)}_{qbr_1r}, n^{(1)}_{qbr}, n^{(1)}_{qbw}, n^{(1)}_{qbr_1w}, n^{(1)}_{qbr_2w}, n^{(1)}_{qbw_1r}, n^{(1)}_{qbw_1r_1r}, \ldots, n^{(M)}_{qbr_1r}, n^{(M)}_{qbr}, n^{(M)}_{qbw}, n^{(M)}_{qbr_1w}, n^{(M)}_{qbr_2w}, n^{(M)}_{qbw_1r}, n^{(M)}_{qbw_1r_1r})$$

where

$n_{r_jw_k}$ = the number of processors accessing j read - k write memory modules

$n^{(i)}_{qr_jw_1w}$ = number of processors who want to but can not write in ith j read -one write memory modules because of the memory module conflict

$n^{(i)}_{qr_2w_k r}$ = number of processors who want to but can not read from ith two read - k write memory modules because of the memory module conflict

$(j=0,1,2 \quad k=0,1)$

$n^{(i)}_{qbr_jw}$ = number of processors who want to but can not write in ith j read memory module because no bus is available .

$(j=0,1,2)$

$n^{(i)}_{qbr_jw_kr}$ = number of processors who want to but can not read from ith j read -k write memory module because no bus is avail

$(j=0,1 \qquad k=0,1)$

$(n_{r0w1}=n_{w1}, n_{r1w0}=n_{r1}$ etc.)

By using the above assumptions and system state, A state transition diagragh can be drawn. And then the equilibrium probabilities of the states can be calculated based on numerical analysis, Lastly. we can obtain processing power by using the calculated probabilities. As an example, the processing power of 3*(2-2)* 2 system is shown in figure 2.

4. Results

We can see from figure 2 that the system with copied memories obtains an obvious perfpormance improvement over against the systems without copied memories. Much more improvement can be expected if the number of global buses and processors increases .

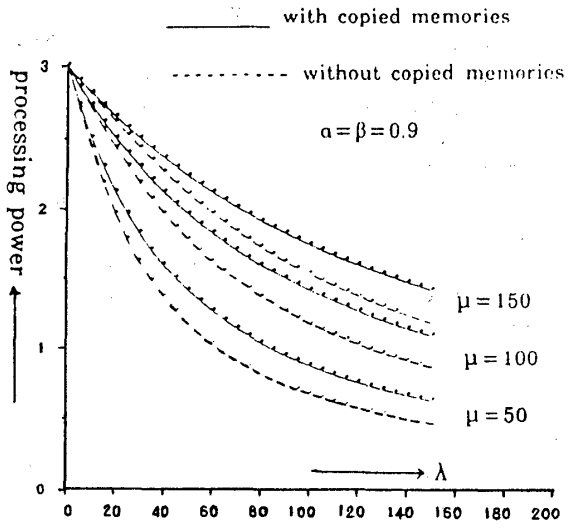

Figure 2 A Comparasion of performance between Multiprocessor Systems with and without Copied Memories

References :

1.Marco Ajmone Marsan & Mario Gerla "Markov models for multiple bus multiprocessor systems" IEEE Trans on Computers, Vol. C-31, No.3 Mar. 1982

2. Marco Ajmone marsan, Gianfranco Balbo, & Gianni Conte "Comparative performance analasis of single bus multiprocessor architectures" IEEE Trans on Computers,Vol C-31 No.12, Dec. 1982