System Design of ETL MK-4B, an Input-Output Computer

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1. *Introduction*

ETL MK-4B now under development is a special purpose computer which cooperates with the master computer, ETL MK-4A, in processing input-output data. However, MK-4B is not a simple data synchronizer because it has a 1,024-word memory and can also operate as an ordinary stored-programmed computer independently of the master computer. The main reason for adopting such a combined system was the fact that the latter was not constructively suited to provide furthermore additional input-output devices.

2. *System Organization*

MK-4B is a parallel binary computer with 32-bit word length. The internal memory is a word-organized ferrite core matrix with 1,024 words and 10 μs cycle time. One word contains a pair of instructions which are of the single address type, or a fixed point, signed-fraction number or four characters with 8 bits each.

One of the outstanding features of MK-4B is the ability of executing several operations simultaneously in order to increase the effective speed of the computer. Fig. 1 shows schematically the principal registers and information paths between them.

Instructions are placed in the Instruction Register T in the Main Control Unit during the instruction memory cycle. During the next operand memory cycle, an operand is transferred between the memory Register M and the other registers; A, B, D, P_1, P_2, J, S.

The A and B Registers in the Arithmetic Unit are of full word size and hold data words for the arithmetic or logical operation. The D Register in the Arithmetic Unit and the two P Registers in the Magnetic Tape Control Unit are of half word size and are used as auxiliary instruction registers in which control words are placed. Once a control word is transferred to an auxiliary instruction register, it is decoded in the respective unit and the several operations are executed independently of the Main Control Unit. Therefore, at some time an instruction and three control words may be simultaneously manipulated in the Main Control Unit, the Arithmetic Unit and the Magnetic Tape Control Unit respectively.

The J Register in the Interrupter Unit is also of half word size and

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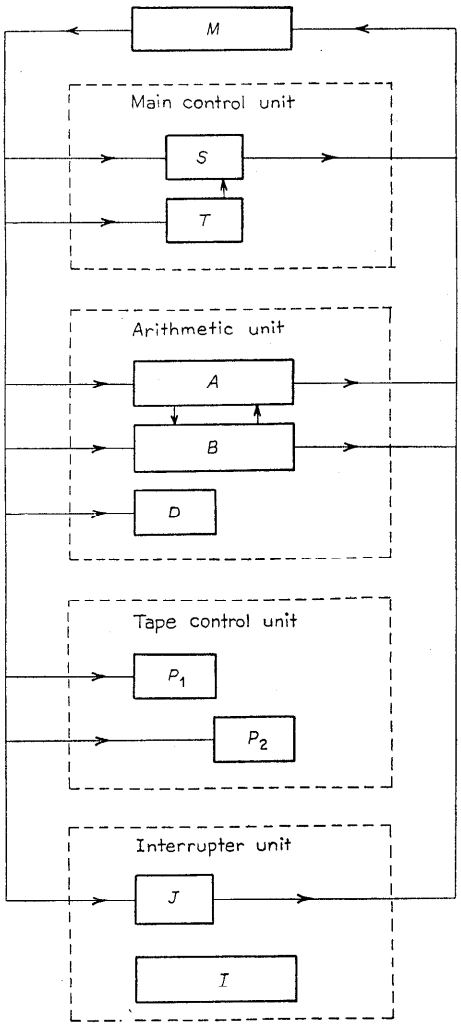

FIG. 1. Principal Registers and Information Paths between them.

is used as a mask register for the Indicator Register I. The Indicator Register consists of several flip-flops indicating the status of the input-output devices. The program interruption scheme by means of these registers is described in the next section. The *S* Register is a sequence control counter.

The computer communicates with the input-output devices through the 8-bit input and output buffers. No other special buffer registers are provided. The input-output devices, currently scheduled for the connection to MK-4B, include four magnetic tape handlers, a high speed line printer, a paper-tape punch and photo-electric paper-tape readers.

3. *Time-Sharing Scheme*

The most important method for increasing the effective speed of the computer is to eliminate unnecessary waiting time in the respective units. Therefore it is highly desirable for several operations to be performed on the time-sharing basis causing the program interruption.

The program interruption scheme of MK-4B is shown schematically in Fig. 2. Although the Indicator Register consists of more than independent 16 flip-flops, the required flip-flops for a run are selected through the plugboard in the control console. These flip-flops are set on if the corresponding input-output devices are busy. If any flip-flops in the Indicator Register are off and any one of the corresponding program-set bits in the Mask Register is "1", the first condition on the interruption is met.

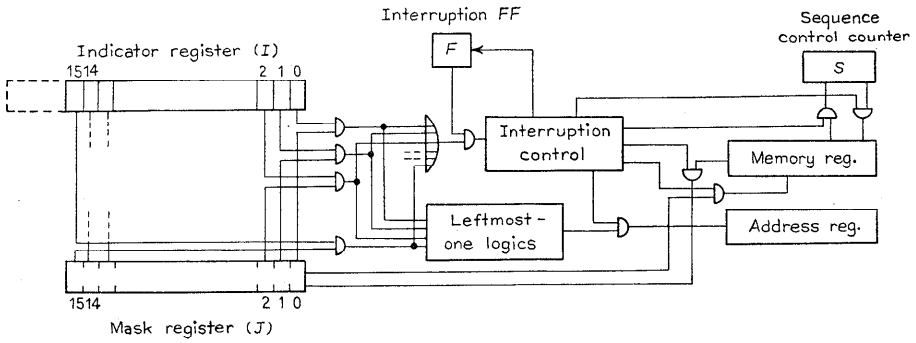

FIG. 2. Program Interruption Scheme.

The interruption flip-flop F controls the over-all operations of the Interrupter Unit. The program interruption can occur only when this flip-flop is on and the first condition is also met. Once an interruption is initiated, the flip-flop F is reset and automatically set agin immediately after the completion of the interruption.

In the case that more than two indicator flip-flops filtered by the Mask Register are simultaneously off, the leftmost one of the indicator flip-flops takes the highest priority among them. A particularly reserved storage location is selected by the built-in leftmost-one logic. The contents of the sequence control counter and the Mask Register which are of half word size each are stored into this reserved location. Successively, the right-half and left-half contents of a different, reserved storage location are placed in the sequence control counter and the Mask Register respectively. Therefore this operation causes the program interruption and switches the current program to a required one. During these operations the flip-flop F is off, so that another interruption cannot be

caused and at the end of the interruption the flip-flop is automatically set on again.

The automatic replacement of the content of the Mask Register enables the jumped sequence to select a necessary mask upon interruption. After the automatic interruption is completed, the contents of the arithmetic registers are usually stored at the initial part of a program sequence and revived at the final part of the program.

Furthermore the memory interruption without altering control can always be caused at the end of both memory cycles. The priority among the different demands is established with a bult-in circuit. The demand from the Magnetic Tape Control Unit takes the highest priority and the one from the Main Control Unit takes the lowest one.

4. *Connection to MK-4A*

Information transfer between MK-4B and MK-4A is carried out as follows: (1) Data words are transferred between their memories (2) Control information between them is transferred through a flip-flop.

The storage locations of MK-4B are also addressable from MK-4A. If the output data are required to be printed out at the side of MK-4A, a series of data are first placed into the output area of the MK-4Bś memory from that of the MK-4Aś. Secondary, a flip-flop which is located in MK-4A and is considered to be an indicator flip-flop to MK-4B, is set on. An instruction of MK-4A in such a case is "test a flip-flop and if it is on, jump to n location, otherwise set a flip-flop". The flip-flop causes the program interruption to MK-4B and an output subroutine is executed. After the completion of the subroutine MK-4B resets the flip-flop. During these operations in MK-4B it is entirely unnecessary for MK-4A to take care of printing out the data.

5. *Conclusion*

Since the authors had no experience in the use of multiprogrammed system, we choosed the one as flexible as possible. From a different point of view it may be said that some ambiguity still retains in the programming techniques, we shall reconsider the system after examining programs of practical problems. The authors wish to acknowledge the contributions of several colleagues: Y. Kato, H. Aiso, K. Kondo, J. Abe.