OSACA;A System for Automated Routing on Two-layer Printed Wiring Board

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1. Introduction

The recent advancements of design techniques for printed wiring boards make the interconnection density higher and higher, and the cost of packing a digital system has become more expensive than that of the components themselves. Thus, an efficient automated design system of printed wiring boards is of primary importance[1].

This paper describes a software system for interconnection routing on two-layer printed wiring boards; OSACA(Organized System for Automated Connection-routing Algorithm) which consists of three different routing algorithms so that the advantage of one may compensate for the defect of another. Fig.1 shows the general flowchart of the system OSACA.

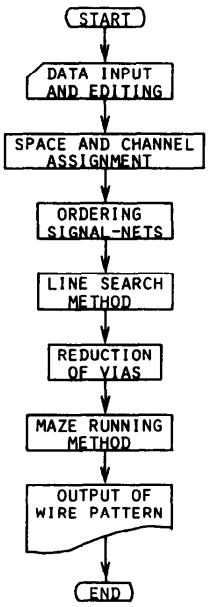

Fig.1 General flowchart of OSACA

2. Preliminaries

We divide the board area effective for wiring into X columns and Y rows, both with the same width of 1.27 mm (1/20 inch). Let each of the X×Y square regions thus obtained be called an f-mesh (fine mesh), and the set of all f-meshes on the same column (or row) is called a vertical channel (or a horizontal channel).

The circuit modules to be mounted are classified into the following classes: (1) s-IC ; a standard IC that is a dual-in-line package IC with 14,16 or 18 pins: (2) o-IC ; a dual-in-line package IC other than an s-IC or a circuit module whose pins are arrayed in a dual-in-line: (3) TM ; an I/O terminal whose pins are located in a line at one of the four sides of the board: (4) OM ; a circuit module other than any of

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those listed above.

A signal-net is a set of pins to be made electrically common. We designate a special signal-net, for which a user wants to preassign the conductor route, as a signal-net with first priority. A signal-net without first priority, which includes a pin of a circuit module in TM, is called a signal-net with second priority, and any one not mentioned above is a signal-net with third priority. For convenience, we denote by S_n a set of signal-nets which are with nth priority.

We divide the effective area of the board into m columns and n rows such that the number of vertical channels in each column is [X/m] or [X/m]+1, and so with each row. Let each of the m×n rectangular regions thus obtained be called a block. Furthermore, each block is subdivided into 3 columns and 4 rows; then each rectangular region thus obtained is a set of f-meshes, which we call an s-mesh (space mesh). As for this subdivision, a block consists of twelve s-meshes so that an s-IC with 14 pins is just mounted on the middle two s-meshes of a block. The set of all s-meshes on the same column (or row) above-mentioned is called a vertical space (or a horizontal space).

3. Connection algorithm

3.1 Space and channel assignment

The first algorithm is space and channel assignment, henceforth abbreviated by SC ,which is made up of the space assignment and channel assignment.

The space assignment is to breach each conductor route between two given pins into a set of horizontal and vertical segments, and then to assign these segments to appropriate horizontal and vertical space. Meanwhile, the channel assignment determines the absolute position of each segment on the board. This procedure is independently applied to each space. The application of the chaanel assignment to each horizontal or vertical space yields the assignment of all the segments in the space to the minimum number of channels. Both ends of each segment are specified by the axial co-ordinates of two segments, and one is connected to the other at each end.

3.2 Line search method

The line seach method is essentially for determining a route between two f-meshes by searching horizontal and vertical segment candidates which may construct a required route. We introduce a restricted line search method, henceforth abbreviated by LS, which is developed to be incorporated into OSACA.

It is the distinctive feature of LS that the application of LS for two f-meshes

yields a route connecting them which consists of three or less horizontal segments and two or less vetical segments whenever such one exists. The restriction to seach for such a limited class of routes enables us to preclude a great amount of search procedure to be wasted until it is ascertained that such a route can not be found.

If a signal-net is composed of three or more pins, then we must provide a procedure for seeking a route connecting an isolated f-mesh and a segment group, i.e. a set of the segments which have been so far constructed. LS is modified so as to be applied to this case.

3.3 Maze running method

The maze running method is to find one of the shortest routes between two specified f-meshes whenever one exists. Basically, this algorithm consists of two processes. One is to seek a route by means of expansion of the search area around the starting f-mesh until the target f-mesh is reached. The other one is to determine the route backward from the target to the starting f-mesh by tracking in the reverse order of the search so far conducted. This approach was proposed by many authors; and, yet, it should be noted that none of these procedures gives any concrete policy about the case when three or more pins are to be connected.

A distinctive feature of MZ is to deal with one incompleted signal-net, which may be partially connected, at a time. In the searching process, we start from one of the connected segments of the net and search adjacent f-meshes one by one. Thus, the application of MZ to an incomplete signal-net yields those conductor routes which form a tree connecting all the pins in the signal-net, whenever such one exists.

4. Implementation description

4.1 Ordering schemes for signal-nets

We discuss here an applying sequence of signal-nets with the same priority. Consider a signal-net N_i, whose isolated pins are in n_i distinct circuit modules, each of which is in an s-mesh $[x_j,y_j]$* $(1 \le j \le n_i)$. The three functions for N_i are defined as follows:

$$f_1(i) = n_i + \alpha_i \ ;$$

$$f_2(i) = (\mathrm{Max}_j\ x_j - \mathrm{Min}_j\ x_j) + (\mathrm{Max}_j\ y_j - \mathrm{Min}_j\ y_j) \ ;$$

$$f_3(i) = |x_0 - 1/2(\mathrm{Max}_j\ x_j + \mathrm{Min}_j\ x_j)| + |y_0 - 1/2(\mathrm{Max}_j\ y_j - \mathrm{Min}_j\ y_j)| \ ;$$

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* An s-mesh in column x and row y is denoted by [x,y], where the origin [1,1] is at the bottom left-hand corner of the board.

where α_i=1 if a pair of pins of N_i is connected by means of SC, and otherwise α_i=0, and $[x_0,y_0]$ is an s-mesh of the center of the board.

Using these three functions, we introduce a priority for N_i by means of triplet function $F(i) = (f_1(i),f_2(i),f_3(i))$. Now we decide the order of dealing with the signal-nets as follows; if $F(i) < F(j)$, then N_j is to be dealt with before N_i, where the ordering of F(i) is lexicographic order. The implemented results show that this ordering scheme can be applied with much property.

4.2 Applying limits of SC, LS and MZ

The applying limits for the algorithm SC, LS and MZ are outlined as follows:

SC : Select a pair of pins for each signal-net on S_3. If such pins are found in a signal-net, SC tries to determine a route between them; otherwise under a certain criterion SC does not deal with this signal-net.

LS : (1) Deal with the signal-nets in S_1 in the order of input by user. (2) Deal with the signal-nets in S_2 in the order described in the previous subsection. (3a) Seek a route between a pair of pins at the longest rectilinear distance for each signal-net in S_3, with which SC did not deal. (3b) Try to complete the signal-nets, which have three or more pins, in S_3 in the order described in the previous subsection.

MZ : Try to accomplish the interconnection of incomplete signal-nets in the same order as in LS.

4.3 Some results of OSACA[2]

Table 1 shows the implemented results of two examples. It also shows the results of APD (Automatic Printed-Circuit-Board Design ; is a program of Nippon IBM Co., Ltd.) in order to recognize the scale of these examples. Because of difference of input schemes between two systems, there is a little modification of the placement of circuit modules in OSACA; but the data of signal-nets and board size are the same.

5. Conclusion

In OSACA, LS is considered as the main routing algorithm; and SC and MZ help LS with their distinctive features. We know that to complete the interconnection between two pins is more difficult than that between a pin and a segment group. By this reason SC, in advance of LS, tries to accomplish a connection between the properly chosen two pins in each signal-net in S_3; and in this sense, SC may be considered as a supplementary algorithm for LS. Meanwhile, MZ supports LS, in a sense that MZ tries to accomplish those signal-net which were not completed by LS (or SC) more minutely and

Table 1

Input data

EXAMPLE NUMBER	SIZE (f-mesh)	CIRCUIT MODULES					NUMBER OF SIGNAL-NETS
		TM	s-IC	o-IC	OM	total	
1	230×120	4	34	2	24	64	144
2	234×125	4	29	19	5	57	271

Implemented results

EXAMPLE NUMBER	SYSTEM	NUMBER OF VIAS	NUMBER OF SEGMENTS	WIRING RATE			
				sc	ls	mz	total
1	APD	329	961	– %	97.53%	2.19%	99.72%
	OSACA	405	895	8.20	90.98	0.82	100
2	APD	833	1839	–	70.38	17.95	88.33
	OSACA	794	1614	5.18	88.21	4.29	97.68

widely.

Thus, OSACA displays its ability with three different algorithms organized as described above; especially when the requirement for high density packing on large board is desired.

References

[1] M.A.Breuer (ed.); Design Automation of Digital Systems, vol.1, pp.420, Englewood Cliffs, N.J., Prentice-Hall, 1972.

[2] A.Sakamoto, T.Chiba, I.Shirakawa, H.Ozaki, S.Sugita, T.Kurimoto, I.Nishioka, "OSACA:A system for automated routing on two-layer printed wiring boards", USA-JAPAN Design Automation Symposium '75, pp.100-107, 1975.