Methods of Wiring Check and Evaluation of their Validity

Yoshiaki KOGA* and Isao SASAKI*

Abstract

In this paper, a selection of the input terminal to minimize the number of wires masked by a certain disconnected wire is presented first for efficient test procedures; and it is shown that an input terminal should be selected as the center of wiring moment. A step-by-step checking method and an AND/OR gate checking method are presented secondly for an automatic wiring check to locate multiple discontinuity failures on wires, and several testing algorithms are shown. In the setp-by-step checking method, it becomes clear that the failure modes are closely related to the test procedures, and the high effectiveness of the AND/OR gate checking method for fault location is proved by computer simulation.

1. Introduction

An automatic wiring check before assembling parts is important for assuring high reliability of digital equipment. A logic circuit network is represented by a directed graph, but a wiring network is represented by an undirected graph; then an arbitrary terminal can be selected as an input terminal for testing. Wiring tests are different from the fault diagnosis of logic circuit networks. This means that multiple failures are possibly located in wiring diagnosis. In place of the test method of using bell- check with wiring diagrams and heuristics, the test method of using automatic wiring test equipment, such as Flexible Automatic Circuit Tester (FACT), has been widely used in wiring check. A test procedure algorithm for this wiring check equipment is the point-to-point checking method similar to the bell-check method. Behavioral and structual testing have been presented as failure detection methods by means of a sequence of multiple-probe continuity tests by W.H. Kautz, but still there are several unsoleved problems in wiring check; for example, selection of input terminals for testing efficiently, failure location and so on.

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* Department of Electrical Engineering, National Defense Academy

In this paper, a selection method of test input to minimize the number of untested wiring to avoid masking effect is discussed first. In wiring check methods, a step-by-step checking and an AND/OR gate checking methods are presented next as failure location methods for the purpose of reducing the number of tests. In these methods, failures of a cluster with arbitrary terminals connected together internally are located from external terminal tests. Failure detection tests are used together to reduce the number of tests. Fundamental functions of test equipment, test algorithm and relation between the number of failure modes and the number of tests will also be related to each other. Validity of the above testing methods will be evaluated by computer simulation.

2. Selection method of an input terminal for wiring check

Selection rules of an input node for the wiring test method to use one test input will be presented. Selection of an input node for a test signal is important to avoid its signal masking by failures of specific wires and to transmit the test signal to as many as possible to test efficiently. So it is necessary to select a suitable input node before reduction of the number of tests and reduction of processing test results. Two selection methods, that is, to select an input terminal in local and to select an input terminal in global, will be considered.

2.1 The maximum degree point method (MDP method) A node of the maximum number of edges connected directly with an input node is selected as the input node. In this manner, the node of the maximum degree becomes an adjacent node to input, and the external terminal on the node becomes the input node. The number of masked wires by failure is expected to be small because many edges are connected with the adjacent node to input. However, the input node selected by this method is not always a suitable node for efficient wiring tests. So another selection method in global will be discussed next.

2.2 The moment method (MOM method) Let a distance between node v_i and v_j on a tree graph $G = (V, E)$ be $d(v_i, v_j)$, and assign one weight to each other, where V is the node set, and E is the edge set. Let a node on the subtree $G' = (V', E')$ of G be v_i'. The moment $M(v_0)$ arround the adjacent node v_0 ($\notin V'$) to arbitrary node v' on V' is given by

$$M(v') = \sum_{v_i' \in V} d(v_0, v_i') \qquad (2.1)$$

As the moment of tree type wiring is equivalent to the number of edges masked by

failures, the node of the minimized moment of tree type wiring should be selected as the input node for the purpose of minimization of the number of masking edges.

$$F(v_0) = \min \sum_{v_i \in V_\alpha} d(v_0, v_i) \qquad (2.2)$$

$$V_\alpha \cup \{v_0\} = V.$$

The node v_0 is called the center node of the moment, and the node set of v_0s is called the center of the moment. Consequently, an adjacent node to input is the center node of the moment, and the external on the adjacent node to input, is the input node. It becomes clear that the center node of the moment minimizes the influence of masking in wiring check. It will take much calculation time to obtain the center of the moment, then a simple procedure to obtain nodes of the near center of the moment will be shown as follows.

Step 1 δ(control variable)$\leftarrow$0 and select an arbitrary node v_t on the tree graph T.

Step 2 Make a path P between arbitrary nodes v_i and v_j through v_t and max $d(v_i, v_j)$. $\delta \leftarrow \delta + 1$, $M\delta \leftarrow \delta$.

Step 3 Obtain node v_δ (there always exist one or two nodes on one path) to minimize the moment for nodes on P.

Step 4 Remove the node v_δ temporarily. If there exist subtrees T_α that contain no edge on P in disjoined subtrees, then go to step 5; otherwise, go to step 6.

Step 5 If $\alpha \geq 2$, then go to (1) otherwise go to (2).

(1) Composit the subtree T_α connected at node v_δ with an arbitrary pair of subtrees T_α. $v_t \leftarrow v_\delta$, and let arbitrary nodes be v_i and v_j again. Go to step 2.

(2) Let the node on T_α be v_i. $v_t \leftarrow v_\delta$, $v_j \leftarrow v_\delta$. Go to step 2.

Step 6 Apply equation (2.2) to node v_δ (δ= 1,2,...Mδ) and select the center node v_c.

3. Wiring check methods for failure location

In wiring check, test equipment is assumed to have the following fundamental functions. (1) If failures exist, test equipment can skip from a normal test to a failure location test. (2) If no failures exist, test equipment can continue the normal test. (3) Test equipment can detect failures on many edges from output terminals of tested wires by using AND operation or OR operation, and can locate a

failure of an arbitrary edge by using their operation (Fig. 1).

3.1 The step-by-step test method The step-by-step test method is a sequential test method based on wiring modes and failure modes of transmission line. A test generation method will be given in the same way that it was used previously[2] to list up all possible failure modes. The test procedure of a three terminal transmission line(n=3) is shown in Fig.2 as an example. This test generation method exactly follows the failure mode analysis algorithm, and the total number of tests is induced

$$p(n)=\frac{1}{\sqrt{5}}\left\{\left(\frac{1+\sqrt{5}}{2}\right)^{2n-1}-\left(\frac{1-\sqrt{5}}{2}\right)^{2n-1}\right\}-1 \qquad (3.1)$$

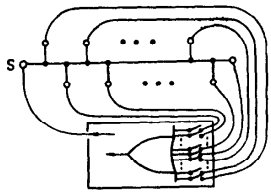

Fig. 1 OR operation of test equipment

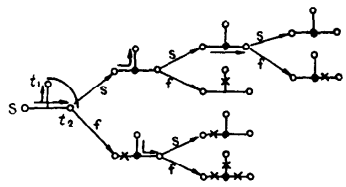

Fig. 2 Step-by-step test(n=3)

3.2 The AND/OR gate test method Terminals on wires under test are grouped together for efficient testing. Two methods for failure location using grouping test are considered. (1) Tree type wiring is devided into two groups as shown in Fig. 3 for a failure location method. AND operations perform for every group, the results of logic operations perform for every group and failure location will be estimated. (2) OR operation is performed for output signals in multiple groups if failures are detected by AND operation as shown in Fig. 4. The first method can locate easily in case of single failure, but multiple failures location may be much more complicated. The second can determine a failure or no failure on a specific edge by discrimination of an output signal of OR gate, and is not influenced by multiple failures on others parts. Therefore, the latter method is more powerful for multiple failure location test. Several grouping method dividing test outputs for test evaluation are given as (a) the branch grouping method (b) the equivalent weight grouping method and (c) the equivalent output terminal grouping method.

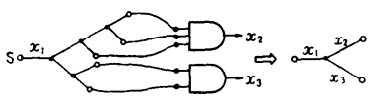

Fig.3 A method of failure location by using AND gates

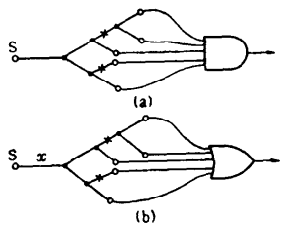

Fig.4 A failure location method by using AND/OR gates

4. Evaluation of the validity of the wiring test method

The above AND/OR gate method has been simulated by a computer for evaluation of its validity. Simulation of a test has been excuted in substance as follows. (1) Tree type wiring is represented by a modified vertex matrix, and failures are generated randomly in the matrix. (2) A test is generated by a test procedure generating method. (3) Tests are performed on the basis of the AND/OR gate test method, and the number of tests for failure location and maintenance imformation are given. Twenty different tree type wiring have been generated for simulation. An example result is shown in Fig. 5. The average numbers of tests in all tested wiring is shown in Fig. 6 for comparison with the failure location by the point-to-point test method. The cross-over point is shown in Fig. 6, as the failure rate is about 25%, and the actual failure rate should be small enough; then the AND/OR gate test method will be the efficient test method.

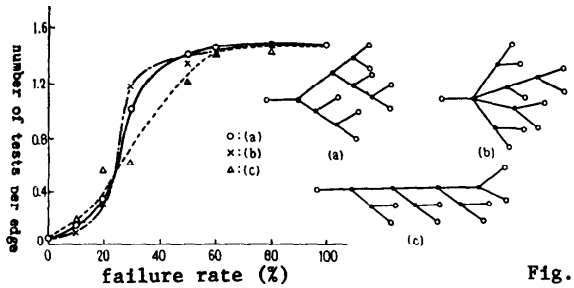

Fig. 5 simulation results

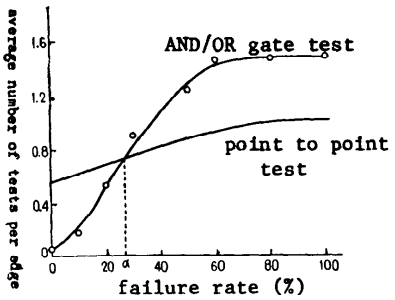

Fig. 6 Comparison of average numbers of tests.

5. Conclusion

Theoretical analysis of wiring modes and failure modes for wiring checks were investigated in reference (2). In this paper, a selection method of an input node has been discussed from the viewpoint of efficient test procedures. As a result, a few rules for a systematic wiring test have been found; and it has been denoted that the center of the moment is suitable for the input node of the test signal.

Failure location methods for clusters have been presented. It has been made clear that there exists a close relation between the number of failure modes and the number of tests, and that the AND/OR gate test method is less in number of tests and is effective for actual use.

References

(1) Y. Koga, A checking of wiring, 7th Design Automation Workshop Proceedings pp 173-177, 1970

(2) Y. Koga and I. Sasaki, Theoretical analysis of wiring modes and failure modes for automatic wiring check, JIPSJ Vol. 16, No. 1, pp 30-38, 1975