設計自動化 38-4
(1987・7・23)

カスタム集積回路コンファレンス(CICC87)から

浅田 邦博

東京大学・工学部

本年5月上旬に米国オレゴン州ポートランドで開催された第9回のカスタム集積回路コンファレンス(CICC87)について紹介する。本会議は教育セッション1日を含めて4日間開催された。学術セッションは4並列で構成されており基調講演を含めて161件の講演と3つのイブニングパネルがもたれた。これらの講演の中で日本および欧州からの参加はそれぞれ21件と22件であった。また基調講演で象徴された今回のテーマはUSIC(User Specific Integrated Circuits)ということであった。

A Short Review of Custom Integrated Circuit Conference (CICC'87)

Kunihiro ASADA

Department of Electronic Engineering, The University of Tokyo
7-3-1 Hongo, Bunkyo-Ku, Tokyo 113 Japan

This is a short review of the 9th Custom Integrated Circuit Conference (CICC'87) held in Portland (Oregon U.S.A.) early in the last May. The conference consists of one day educational session and three day academic sessions running in four parallels. There were 161 presentations, including a keynote address, 21 and 22 of which were Japanese and European papers, respectively. The "USIC" (User Specific Integrated Circuit) was the conference motif given by the keynote address.

１．会議の概要

第９回カスタム集積回路コンファレンス（ＣＩＣＣ８７）は、本年５月４日から７日までの４日間、米国オレゴン州のポートランドで開催された。表１に示される日程に従い、第１日目の月曜日は教育セッションであり本会議は翌日から木曜日までの３日間であった。会場はポートランド・ヒルトン内の３会場と真向いのミュージック劇場の、計４会場があてられ、４並列セッションのかたちで運営された。会議はT. Foxall (General Chairman)、D. Bryant (Conference Chairman)等らの挨拶に始まり、Technical Program Committee のR. Milanoの経過報告のあと、A. Rappaport の基調講演で開始された。発表件数は基調講演のほか１６０件あり、二日目の夜には、３つのイブニング・セッションがおこなわれた。なお、日本からの発表件数は２１、欧州からは２２であった。

２．基調講演

ボストンのTechnology Research Group のA. Pappaport による基調講演の演題は"The Custom IC Business is Dead, ..." とやや奇抜な印象を与えるものであったが、結論はカスタム集積回路のビジネスを否定するものではなかった。ユーザと応用の２つを直交する軸ととらえ、今後はユーザにより重きをおいたＵＳＩＣ(User Specific Integrated Circiut)を提唱していた。ＵＳＩＣの略語自体は数年前の日経エレクトロニクス誌等にもすでにみられるが、本講演ではやや陳腐化してきた感がある略語、ＡＳＩＣに新風を吹き込む効果を狙ったものとも解釈できよう。

３．一般講演

招待講演を含め一般講演は、設計ツール／手法関係、回路／デバイスのモデリング関係、ＬＳＩ開発報告等のほか製造技術、テスト、信頼性等の多岐に渡っている。表２にプログラムを示す。全般に本会議においても製造技術に関係する分野と民生品に応用可能なＬＳＩ開発報告では日本からの発表に関心がよせられ、半導体摩擦の根本を垣間見た印象を受けた。

なお表１にも示されているように、発表者へのインタビュー時間が夕方に設けられており、これを前提としてセッション間の同期はかなり厳格に行われた。

４．その他

イブニング・セッションでは

(1) Next Generation Layout Tools and Methodologies

(2) Front End Tradeoffs in ASIC Chip Design

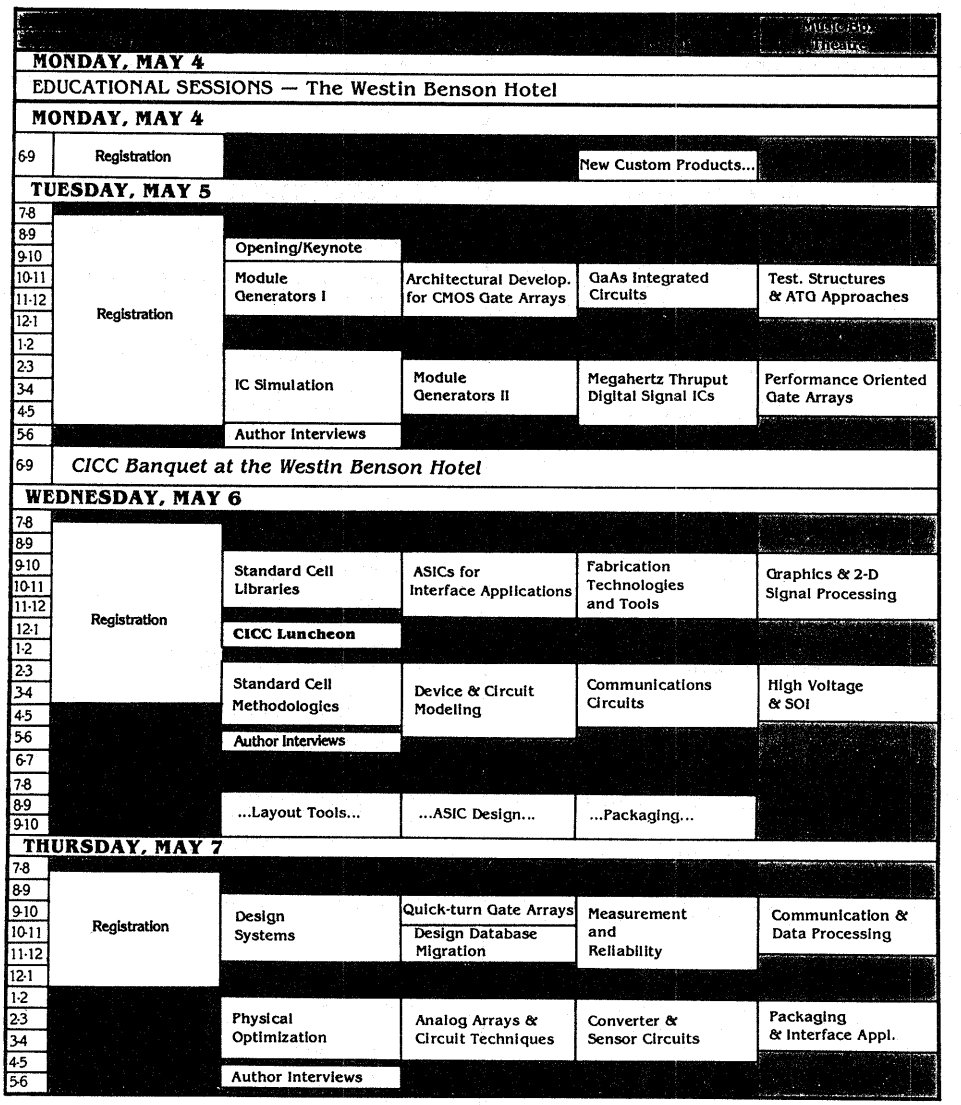
(3) Challenges in Packaging High Performance VLSI Functions

の３つのテーマでおこなわれた。

なお、筆者自身は設計手法に関するセッションに主として参加したが、それらを中心に各セッションの内容については当日報告したい。

TABLE. 1

CONFERENCE OVERVIEW



MONDAY, MAY 4					
EDUCATIONAL SESSIONS — The Westin Benson Hotel					
MONDAY, MAY 4					
6-9	Registration			New Custom Products...	
TUESDAY, MAY 5					
7-8	Registration				
8-9		Opening/Keynote			
9-10		Module Generators I	Architectural Develop. for CMOS Gate Arrays	GaAs Integrated Circuits	Test. Structures & ATG Approaches
10-11					
11-12					
12-1					
1-2					
2-3		IC Simulation	Module Generators II	Megahertz Thruput Digital Signal ICs	Performance Oriented Gate Arrays
3-4					
4-5					
5-6		Author Interviews			
6-9	*CICC Banquet at the Westin Benson Hotel*				
WEDNESDAY, MAY 6					
7-8	Registration				
8-9					
9-10		Standard Cell Libraries	ASICs for Interface Applications	Fabrication Technologies and Tools	Graphics & 2-D Signal Processing
10-11					
11-12					
12-1		**CICC Luncheon**			
1-2					
2-3		Standard Cell Methodologies	Device & Circuit Modeling	Communications Circuits	High Voltage & SOI
3-4					
4-5					
5-6		Author Interviews			
6-7					
7-8					
8-9		...Layout Tools...	...ASIC Design...	...Packaging...	
9-10					
THURSDAY, MAY 7					
7-8	Registration				
8-9					
9-10		Design Systems	Quick-turn Gate Arrays	Measurement and Reliability	Communication & Data Processing
10-11			Design Database Migration		
11-12					
12-1					
1-2					
2-3		Physical Optimization	Analog Arrays & Circuit Techniques	Converter & Sensor Circuits	Packaging & Interface Appl.
3-4					
4-5					
5-6		Author Interviews			

TABLE 2

TUESDAY MORNING — State Room (Hilton)

8:30 WELCOME/OPENING REMARKS

T. Foxall, General Chairman
D. Bryant, Conference Chairman

8:50 CICC '87 - TECHNICAL PROGRAM
R. Milano, Technical Program Committee Chairman

9:00 KEYNOTE ADDRESS
"The Custom IC Business is Dead, Long Live Custom, ICs"
A. Rappapo.
Technology Research Group, Boston, MA

MODULE GENERATORS I
Chairman: ... Barnes
Co-Chairman: J. Allen

9:45 MAP: A Parameterizable Module Generator Development System Oriented to IC Designers
S. Powell, E. Barouch, Hughes Aircraft Co., Carlsbad, CA

10:10 A Flexible-Cell Approach for Module Generation
Y—L.S. Lin*, D.D. Gajski*, H. Tago**, Univ. of Illinois, Urbana IL*, Toshiba Corp., Kawasaki, Japan**

10:35 An Optimizing XROM Silicon Compiler
P.C. Rossbach, R.W. Linderman, D.M. Gallagher, Air Force Institute of Technology, Wright-Patterson Air Force Base, OH

11:00 Crystal Oscillator Compiler
J. Lach, Seattle Silicon, Bellevue, WA

11:25 A MOS Leaf-Cell Generation System from Boolean Expressions
K. Asada*, J. Mavor**, Univ. of Tokyo, Tokyo, Japan*, Univ. of Edinburgh, Edinburgh, United Kingdom**

11:50 Complex MOS Gates Compiler
G. Thuau, G. Saucier, INPG, Grenoble, France

12:15 LATE PAPER
"ASIC Designs using VITAL"
R.H. Dawson, B.J. Witkosky, S. Kotcherlakota, RCA, Somerville, NJ

TUESDAY MORNING — Rose Room (Hilton)

ARCHITECTURAL DEVELOPMENTS FOR LARGE CMOS GATE ARRAYS

Chairman: H. Scalf
Co-Chairman: M. Hollabaugh

9:45 A 0.5 Micron 150K Channelless Gate Array
F. Anderson, J. Ford, Motorola, Inc., Phoenix, AZ

10:10 Advanced Structured Arrays Combine High Density Memories with Channel-Free Logic Array
T. Chan, A. Yuen, K. Knorp, M. Hung, P. Tsao, M. Freie, Y. Chang, R. Rasmussen, A. Hui, P. Yin, LSI Logic Corp., Milpitas, CA

10:35 Effective Implementation of Complex and Dynamic CMOS Logic in a Gate Forest Environment
M. Beunder, J. Kernhof, B. Hoefflinger, Institut for Mikroelectronik, Stuttgart, West Germany

11:00 Layout Approaches to High-Density Channelless Masterslice
H. Kubosawa*, G. Goto*, S. Tsutsumi**, Y. Sudhiro**, T. Sanato**, Fujitsu Laboratories Ltd., Atsugi, Japan*, Fujitsu Ltd., Kawasaki, Japan**

11:25 Triple-Level Metal Gate Array using Channelless Architecture
K.Y. Liao, C-P Hsu, M-R Lin, Hughes Aircraft Co., Newport Beach, CA

11:50 An 18K 1 μm CMOS Gate Array with High Testability Structure
M. Kawashima*, M. Takechi*, K. Ikuzaki*, K. Kishida*, K. Itoh*, M. Fujita*, T. Nakao**, I. Masuda***, Hitachi, Ltd., Tokyo, Japan*, Hitachi Ltd., Kanagawa, Japan**, Hitachi Ltd., Ibaraki, Japan***

TUESDAY MORNING — Music Box Theatre

TESTABILITY STRUCTURES AND ATG APPROACHES

Chairman: M.G. Moon
Co-Chairman: S. Hao

9:45 Testability in the TMS34010 Graphics Systems Processor
G. Short, J. Turek, D. Roskell, R. Simpson, Texas Instruments Ltd., Bedford, England

10:10 Logic Verification and Production Testing of Non-Structured Embedded VLSI Blocks
T.G. Breitenwischer, National Semiconductor Corp., Santa Clara, CA

10:35 Automation of BIST for Embedded RAM
D.R. Aadsen*, S.K. Jain**, AT&T Bell Labs, Allentown, PA*, AT&T Bell Labs, North Andover, MA**

11:00 High Fault Coverage Self-Test Structures for CMOS ICs
D.L. Liu, E.J. McCluskey, Stanford Univ., Stanford, CA

11:25 The F-Path Method of Test Generation for Datapath Logic
S. Freeman, RCA Labs, Princeton, NJ

11:50 PROTEAN—A Knowledge Based Test Generator
P. Varma*, Y. Tohma**, HRC, Middlesex, U.K.*, Tokyo Inst. of Technology, Tokyo, Japan**

TUESDAY MORNING — Pavilion (Hilton)

GaAs INTEGRATED CIRCUITS

Chairman: D.F. Perkins
Co-Chairman: S.H. Chiao

9:45 A Monolithic GaAs Error Detection and Correction Circuit for Triple Modular Redundancy Applications
N. Kanopoulos, Research Triangle Inst., Research Triangle Park, NC

10:10 A Gallium Arsenide Encoder/Decoder and Laser Diode Driver for High Speed Optical Communication Links
S.F. Nall, C.E. Marchant, General Electric Co., Syracuse, NY

10:35 A 2 GHz GaAs Line Code Error Detection Circuit for Fiber Optic Communications
B.O. Johannessen*, H.P. Singh**, R.A. Sadler**, A.E. Geissberger**, ITT Corp., Oslo, Norway*, ITT Corp., Roanoke, VA**

11:00 A 1.5 GHz Programmable Divide-by-N GaAs Prescaler
M.G. Kane, P.Y. Chan, D.C. Fowlis, Microwave Semiconductor Corp., Somerset, NJ

11:25 GaAs Standard Cell Family Designed with Current Limiting Capacitor Diode FET Logic Approach
P.M. Lau, R.C. Eden, F.S. Lee, GigaBit Logic, Newbury Park, CA

TUESDAY AFTERNOON — State Room (Hilton)

IC SIMULATION

Chairman: P. Lloyd
Co-Chairman: C. Anagnostopoulos

1:35 Manufacturing Based Simulation: An Overview
S.W. Director, Carnegie Mellon Univ., Pittsburgh, PA

2:25 Hadamard Simulation—An Effective, Systematic Tool for Worst Case Circuit Analysis
F. Severson, S. Simpkins, Tektronix, Inc., Beaverton, OR

2:50 Parallel PISCES
R. Lucas, T. Blank, Stanford University, Stanford, CA

3:15 Circuit Simulation on a Multiprocessor
P. Sadayappan*, V. Visvanathan**, Ohio State Univ., Columbus, OH*, AT&T Bell Labs, Murray Hill, NJ**

3:40 SAMO: An Automatic MOS Circuit Partitioner
Y-T Yen, K.A. Sakallah, Digital Equipment Corp., Hudson, MA

4:05 HICE: Hierarchical Circuit Extraction System for Layout Verification
G. Yokomizo, A. Yajima, Y. Okamura, T. Sato, Hitachi, Ltd., Tokyo, Japan

4:30 Full Chip RC Routing Extraction and Delay Analysis
M-C Chang, C-F Chen, M-T Yin, AT&T Bell Labs, Murray Hill, NJ

TUESDAY AFTERNOON — Rose Room (Hilton)

MODULE GENERATORS II

Chairman: J. Lipman
Co-Chairman: J. Buurma

2:00 A CRT Controller Generator
M.S. Kaplan, D.J. Gurney, H-G Nguyen, Silicon Design Labs, Inc., Liberty Corner, NJ

2:25 A Datapath Compiler for Standard Cells and Gate Arrays
J. Rowson, B. Walker, S. Dholakia, VLSI Technology, Inc., San Jose, CA

2:50 Basic Operators to Tailor Application Specific Microprocessor System on Silicon
J.Y. Brunel, J.M. Labrousse, Laboratoires D'Electronique et de Physique Appliquee, Limeil-Brevannes, France

3:15 Cathedral II: Computer Aided Synthesis of Digital Signal Processing Systems
J. Rabaey, J. Vanhoof, G. Goossens, F. Catthoor, H. De Man, IMEC Labs., Leuven, Belgium

3:40 Compiler Generation of A to D Converters
W.J. Helms*, B.E. Byrkett**, Univ. of Washington, Seattle, WA*, Seattle Silicon, Bellevue, WA**

4:05 Expert System for Automatic Mixed Analog Digital Layout Compilation
J. Tronelj*, L. Trontelj*, T. Pletersek*, G. Shenton**, M. Robinson***, K. Floyd***, C. Jungo***, Univ. Edvard Kardelj, Trzaska, Yugoslavia*, IMP Europe, Swindon, England**, IMP, San Jose, CA***

4:30 LATE PAPER
"A 4-Bit Gallium Arsenide ALU Designed With a Compiler"
R.E. Oeter*, M.D., Upton*, R. Eden**; F. Lee**; P. Lau**;
Seattle Silicon Corp., Bellevue, WA*, GigaBit Logic, Newbury Park, CA**

TUESDAY AFTERNOON — Music Box Theatre

PERFORMANCE ORIENTED GATE ARRAYS

Chairman: C. Erdelyi
Co-Chairman: H. Scall

2:00 A 600MHZ 5000 Gate ECL/TTL Gate Array
R.S. Tepper, K. Nootbaar, M.P. Huang, R. Yuan, Applied Micro Circuits Corp., San Diego, CA

2:25 A Performance-Programmable Bipolar Gate Array Family for Building Mainframe Computer Systems
D. Still, D. Baldwin, B. Hoffman, D. Wick, Honeywell, Inc., Colorado Springs, CO

2:50 ECL ASICs for Space Application
A. DiCecca, A. Serafini, Selenia Spazio, S.p.A., Rome, Italy

3:15 A 9100 Gate ECL/TTL Compatible BICMOS Gate Array
L.T. Lin, D.S. Rosky, H.D. Truong, Applied Micro Circuits Corp., San Diego, CA

3:40 High Performance BiMOS Gate Arrays with Embedded Configurable Static Memory
P.S. Bennett, R.P. Dixon, F. Ormerod, Motorola, Inc., Chandler, AZ

4:05 LATE PAPER
A 40 ps High Electron Mobility Transistor 4.1K Gate Array
K. Kajiji, Y. Watanabe, M. Suzuki, I. Hanyu, M. Kosugi, K. Odani, T. Mimura, M. Abe, Fujitsu Labs Ltd., Atsugi, Japan

4:15 LATE PAPER
A 0.45ns 7K HI-BICMOS Gate Array with Configurable 3-Port 4.5K SRAM
Y. Nishio*, F. Murabayashi*, I. Masuda*, H. Maejima*, S. Owaki**, K. Yamazaki**, S. Kadono**, Hitachi Res. Lab., Ibaraki-ken, Japan*, Takasaki Works, Gunma-ken, Japan**

TUESDAY AFTERNOON — Pavilion (Hilton)

MEGAHERTZ THROUGHPUT DIGITAL SIGNAL PROCESSING ICs

Chairman: F. Yassa
Co-Chairman: T. Foxall

2:00 A Wafer-Scale 170,000-Gate FFT Processor with Built-In Test Circuits
K. Yamashita, A. Kanasugi, S. Hijiya, G. Goto, N. Matsumura, T. Shirato, Fujitsu Labs Ltd., Atsugi, Japan

2:25 A Modular Chip Set Implementation of an Associative Comparator
R.J. Inkol, Defence Research Establishment, Ottawa, Canada

2:50 Sparse Canonical Signed Digit FIR Filter
L.R. Tate, RCA, Somerville, NJ

3:15 A 70 Mhz 1.2 Micron CMOS 16-Point DFT Processor
R.W. Linderman, C.G. Shephard, K. Taylor, P. Coutee, P. Rossbach, J. Collins, Air Force Inst. of Technology, Wright-Patterson Air Force Base, OH

3:40 GaAs FIR Median Hybrid Filter
O. Vainio*, M. Sundaram**, S. Long**, Y. Neuvo*, Tempere Univ. of Tech., Tampere, Finland*, Univ. of California, Santa Barbara, CA**

4:05 A High Speed LMS Adaptive Filter
T.H. Bui, RCA, Somerville, NJ

4:30 Microcoded RISC Processor for Calculation of the Vector Wave Equation
J. Diaz, J.W. DeGroat, Air Force Inst. of Technology, WPAFB, OH

WEDNESDAY MORNING — State Room (Hilton)

STANDARD CELL LIBRARIES

Chairman: D. Daly
Co-Chairman: T. Sideris

8:20 Designing a CMOS Standard Cell Library
S. Sunter, Bell-Northern Research, Ottawa, Canada

8:45 A High Performance Scalable Standard Cell Library with True Second Sourcing
G. Buxma*, P. Michel**, T. Kuroda***, GE Semiconductor, Research Triangle Park, NC*, Siemens AG, Munich, W. Germany**, Toshiba Corp., Kawasaki, Japan***

9:10 A Versatile VLSI Design System for Combining Gate Array and Standard Cell Circuits on the Same Chip
R. Homung*, M. Bonneau*, B. Waymel*, R. Piro**, J. Flore**, E. Gould**, J. Martin**, L. McAllister**, S. Tom**, IBM, Corbeil-Essonnes, France*, IBM, Essex Junction, VT**

9:35 A 40K Equivalent Gate CMOS Standard Cell Chip
A.W. Aldridge, R.F. Keil, J.H. Panner, G.D. Pittman, D.R. Thomas, IBM Corp., Essex Junction, VT

10:00 1.3 µm CMOS/Bipolar Macrocell Library for the VLSI Computer
T. Motta*, K. Kurita*, H. Maejima*, M. Iwamura*, S. Tanaka*, T. Bandoh*, A. Hotta**, Hitachi Ltd., Ibaraki, Japan*, Hitachi Ltd., Tokyo, Japan**

10:25 An Expert System Functional Description for Parameterized Cells
V. Rapp, G. Hoelzl, C. Georgiou, Siemens AG, Munich, West Germany

WEDNESDAY MORNING — Rose Room (Hilton)

ASICs FOR INTERFACE APPLICATIONS

Chairman: W.A. Vincent
Co-Chairman: A.K. Sitzars

8:20 High Voltage Custom ICs Using BCDMOS Technology
M.A. Banak*, J.C. Gamme*, M.L. Enzmer*, D.M. Pietruszynski*, A. Ortiz-Conde*, R.A. Furnanage,* R.E. Carey*, B.A. Mangieri**, AT&T Bell Labs, Reading, PA*, AT&T Technology Systems, Reading, PA**

8:45 A 30 V Row/Column Driver for Flat-Panel Liquid Crystal Displays
K. Muhlemann, U. Merki, Faselec AG, Zurich, Switzerland

9:10 A Bi-CMOS Thermal Head Intelligent Driver with Density Controllers for Fulltone Rendition Printers
M. Tsumura*, R. Takeuchi*, I. Shimizu**, Hitachi, Ltd., Ibaraki-ken, Japan*, Hitachi, Ltd., Gunma, Japan**

9:35 Smartpower Motor Driver for Low Voltage Application
D. Cave*, D. Soo*, T. Sakurai**, M. Kojima**, S. Utsumi**, Motorola Inc., Phoenix, AZ*, Nippon Motorola Ltd., Tokyo, Japan**

10:00 A Merged Hall Effect/Power IC
P.R. Emerald, Sprague Electric Co., Worcester, MA

10:25 Dynamic Hysteresis Circuit for High Speed CMOS Devices
Y-I Shin, R. Mooney, T. Fletcher, Signetics Corp., Orem, UT

10:50 Self Terminating Low Voltage Swing CMOS Output Driver
T. Knight, A. Krymm, Symbolics, Inc., Cambridge, MA

WEDNESDAY MORNING — Music Box Theatre

GRAPHICS AND 2-D SIGNAL PROCESSING IN REAL TIME

Chairman: L. Christopher
Co-Chairman: D. E. Brown

8:20 A Single Chip Graphic System
P. Lamoureux, J. Lamarche, D. Frank, R. Torrance, S. Sadler, F. Leveille, Silicart Inc., Montreal, Canada

8:45 A CMOS VLSI Chip for Real-time Centroid Calculation
D.D. Shugard*, J.C. Swartzwelder*, M. Hatamian**, AT&T Bell Labs, Murray Hill, NJ*, AT&T Bell Labs, Holmdel, NJ**

9:10 A Microprogrammable Realtime Video Signal Processor (VSP) LSI for Motion Compensation and Vector Quantization
T. Enomoto, M. Yamashina, T. Kunio, I. Tamitani, H. Harasaki, Y. Endo, T. Nishitani, M. Sato, K. Kikuchi, NEC Corp., Kawasaki, Japan

9:35 A Monolithic Image Edge Detection Filter
N. Vasanthavada, R. Baker, N. Kanopoulos, Research Triangle Institute, Research Triangle Park, NC

10:00 Cascadable One/Two-Dimensional Digital Convolver
R. Arambepola, G. Cheung, V.B. Patel, GEC Research Ltd., Wembley, U.K.

10:25 A 20 ns 256K X 4 FIFO Memory
M. Heshimoto, K. Sasaki, M. Nomura, S. Tamura, K. Komatsuzaki, H. Fujiwara, T. Horizawa, K. Abe, T. Komatsuzaki, T. Tachibana, K. Fujita, N. Kitagawa, Texas Instruments Japan Ltd., Ibaraki, Japan

10:50 A 1 Mb Field Memory for TV Pictures
I. Nakagawa*, S. Matsumoto*, S. Hirata*, N. Kojima*, N. Tanimura*, K. Oishi*, H. Wakimoto*, T.J. Christopher**, D.H. Willis**, S.P. Knight**, R.G. Stewart**, Hitachi Ltd., Tokyo, Japan*, RCA Labs, Princeton, NJ**

11:15 LATE PAPER
2 Chip CMOS Digital TV
S. Suzuki, K. Muramatsu, T. Makino, S. Nose, Toshiba Microelectronics Center, Kawasaki-City, Japan

WEDNESDAY MORNING — Pavilion (Hilton)

FABRICATION TECHNOLOGIES AND TOOLS

Chairman: M. Hartranft
Co-Chairman: S. Kohyama

8:20 A Process Engineers Workbench
A.J. Strojwas, S.W. Director, Carnegie Mellon Univ., Pittsburgh, PA

8:45 **Application and Evaluation of Direct-Write Electron Beam for ASICs**
K. Shiozawa*, M. Fujita*, T. Kase**, H. Hayakawa*, F. Mizuno*, R. Haruta*, S. Okazaki*, Hitachi, Ltd., Tokyo, Japan*, Hitachi, Ltd., Kanagawa, Japan**

9:10 **The Effects of Nitride Layers on Surface State Density and the Hot Electron Lifetime of Advanced CMOS Circuits**
R.T. Fuller*, W.R. Richards*, P.M. Sandow*, Y. Nissan-Cohen**, J.C. Tsang*, General Electric Co., Research Triangle Park, NC*, General Electric, Schenectady, NY**

9:35 **A 600 MHz P-Channel JFET Compatible with an 8 GHz Bipolar Process**
R.E. Johnston, A.Y-C Tang, Tektronix, Inc., Beaverton, OR

10:00 **A VLSI Poly-Bipolar Process with 100 psec Gate Delay**
A.K. Kapoor, F.J. Ciacchella, M.B. Vora, N. Bhandari, N. Shamma, Fairchild, Palo Alto, CA

10:25 **A Novel Triple-Diffused Self-Aligned Bipolar IC Process for High-Speed LSI**
D. Fuoss, T. Yuzuriha, Tektronix, Inc., Beaverton, OR

10:50 **An Optimized 1.0 µm CMOS Technology for a Next Generation Channelless Gate Array**
Y. Ushiku, T. Kobayashi, A. Yoshida, N. Itoh, A. Nishiyama, R. Nakata, Toshiba Corp., Kawasaki, Japan

---

WEDNESDAY AFTERNOON — State Room (Hilton)

STANDARD CELL METHODOLGIES

Chairman: K. Venkateswaran
Co-Charman: K. Au

2:00 **An Automatic Characterization System for Standard Cells**
W. Kao, N. Ansari, K. Chan, Xerox Corp., El Segundo, CA

2:25 **Automated SPICE Characterization of Gate Array and Standard Cell Libraries**
D. Vo, VLSI Technology, Inc., San Jose, CA

2:50 **A Procedure for Automatic Electrical Characterization of Standard Cell and Gate Array Libraries**
J. Hansen, B. Richman, R. Lyngaas, R.S. Kirk, Gould, Inc., Pocatello, ID

3:15 **Automatic Cell Synthesis for ASIC**
W.F. Bridgewater, R.P. Pokala, National Semiconductor Corp., Santa Clara, CA

3:40 **Megafunctions and Megacells for ASIC Designs: A Comparison**
D. Watkins, R. Rasmussen, Y. Chang, LSI Logic Corp., Milpitas, CA

4:05 **Design Methodology of Standard Cell Layout and PLA**
K. Usami, A. Ishii, A. Horie, J. Iwamura, Toshiba Corp., Kawasaki, Japan

4:30 **A New Standard Cell CAD Methodology**
R. Reis, Univ. of Rio Grande Do Sul, Porto Alegre, Brazil

WEDNESDAY AFTERNOON — Rose Room (Hilton)

DEVICE AND CIRCUIT MODELING

Chairman: J.S.T. Huang
Co-Chairman: H.S. Abdel-Aty-Zohdy

2:00 **Optimized Application of Submicron CMOS for VLSI Logic—A Systems Oriented View on Design and Technology**
C.M. Huizer, Philips Research Labs, Eindhoven, The Netherlands

2:25 **Efficient and Accurate Simulation of Micron and Submicron MOS Circuits**
T.A. Grotjohn*, B. Hoelflinger**, Purdue Univ., West Lafayette, IN*, Inst. of Microelectronics, Stuttgart, W. Germany**

2:50 **Short-Channel Effects on MOSFET Terminal Capacitances**
C.T. Yao, I.A. Mack, H.C. Lin, Naval Research Laboratory, Washington, DC

3:15 **An Accurate SPICE MOSFET Model for Digital and Analog Circuit Simulations**
Y-T Chia, G. Hu, Sierra Semiconductor Corp., San Jose, CA

3:40 **A GaAs MESFET Model for Circuit Simulation**
P. George, K. Hui, P. Ko, C. Hu, Univ. of California, Berkeley, CA

4:05 **Carrier-Propagation-Delay (CPD) Models for Bipolar Circuit Simulation**
B.S. Wu*, M.K. Chen*, F.A. Lindholm*, T.W. Jung**, Univ. of Florida, Gainesville, FL*, Harris Corp., Melbourne, FL**

4:30 **Optimization-Based Transistor Sizing**
J-M Shyu*, J.P. Fishburn**, A.E. Dunlop**, A.L. Sangiovanni-Vincentelli*, Univ. of California, Berkeley, CA*, AT&T Bell Labs, Murray Hill, NJ**

4:55 **A Deterministic Algorithm for Automatic CMOS Transistor Sizing**
B.A. Richman*, J. Hansen*, K. Cameron**, Gould, Inc., Pocatello, ID*, Univ. of Idaho, Moscow, ID**

WEDNESDAY AFTERNOON — Music Box Theatre

HIGH VOLTAGE AND SILICON IN INSULATORS

Chairman: P. Zeitzoff
Co-Chairman: M. King

2:00 **SIMOX SOI for Integrated Circuit Fabrication**
H.W. Lam, LAM Associates, Dallas, TX

2:50 **High Voltage CMOS IC with a Novel Diffused Well Structure**
H. Hayama, K. Hirata, H. Sakuma, NEC Corp., Kawasaki, Japan

3:15 **A Low Cost Technology for High Voltage Drivers in a CMOS or NMOS Process**
R.A. Martin, Xerox Corp., Palo Alto, CA

3:40 **A Multichannel 300V Level Translator Chip**
H-Y Tsoi, C. Tsay, A. Rupp, B. Choy, Supertex Inc., Sunnyvale, CA

4:05 **Dielectrically Isolated Intelligent Power Switch**
Y. Ohata, T. Izumita, Toshiba Corp., Kawasaki, Japan

WEDNESDAY AFTERNOON — Pavilion (Hilton)

COMMUNICATIONS CIRCUITS

Chairman: C. Jungo
Co-Chairman: A.D. Milne

2:00 **An Analog Front End for V.22 bis Modems**
P.J. Hurst*, T.J. Glad**, J.J. Ilgner**, G.F. Landsburg**, Univ. of Calif., Davis, CA*, Silicon Systems, Inc., Nevada City, CA**

2:25 **A Programmable CMOS Transceiver with 45dB Automatic Equalization**
V.R. Saari*, D.G. Marsh*, D.J. McGuire**, A. Ganesan**, AT&T Bell Labs, Holmdel, NJ*, AT&T Information Systems, Middletown, NJ**

2:50 **CMOS Analog Front End of a Transceiver with Digital Echo-Cancellation for ISDN**
B. Roessler, E. Wolter, H. Sporer, Siemens AG, Munich, West Germany

3:15 **A CMOS IC for Multichannel Voice/Data Communication Over a Single Twisted-Pair Wire**
R.S. Co, G.A. Watson, R.W. Schalk, K.I. Hsu, Rockwell International Corp.,Newport Beach, CA

3:40 **A Low Noise Switched Capacitor Analogue Front End for a V22 BIS Modem**
D.M. Gee, S.R. Laurenson, GEC Research Ltd., Middlesex, United Kingdom

4:05 **Analog Signal Processor for Mobile Radio Systems**
G. Chiappano*, A. Colamonico*, M. Donati*, F. Maloberti**, F. Montecchi**, G. Palmisano**, Italtel, Milano, Italy*, Univ di Pavia, Italy**

4:30 **A Low-Voltage Analog Signal Processor LSI for Mobile Radiotelephone Systems**
H. Tanimoto*, M. Hayashibara*, T. Kato**, Toshiba Corp., Kawasaki, Japan*, Toshiba Corp., Tokyo, Japan**

WEDNESDAY EVENING — State Room (Hilton)

8:00 **EVENING PANEL**

"Next Generation Layout Tools and Methodologies"

MODERATOR:
T. Sideris
Ford Microelectronics, Inc.

WEDNESDAY EVENING — Rose Room (Hilton)

8:00 **EVENING PANEL**

"Front End Tradeoffs in ASIC Chip Design"

MODERATOR:
J. Lipman
VLSI Technology

WEDNESDAY EVENING — Pavilion (Hilton)

8:00 **EVENING PANEL**

"Challenges in Packaging High Performance VLSI Functions"

MODERATOR:
C.K. Erdelyi
IBM

THURSDAY MORNING — State Room (Hilton)

DESIGN SYSTEMS

Chairman: G. Ledenbach
Co-Chairman: R. Bryant

8:45 **High Performance Custom CMOS Design**
R.H. Krambeck, AT&T Bell Labs, Allentown, PA

9:10 **The ChipCompiler, An Automated Standard Cell/Macrocell Physical Design Tool**
M. Hartoog, D. Bohm, L. Grate, D. Hsu, C. Ng, VLSI Technology, Inc., San Jose, CA

9:35 **VENUS® - An Advanced VLSI Design Environment for Custom Integrated Circuits with Macro Cells, Standard Cells and Gate Arrays**
H.G. Thonemann, M. Kolonko, H. Severloh, SIEMENS AG, Munich, West Germany

10:00 **New Software Tools Improve Design Flexibility Through Integration of Gate Arrays, Standard Cells, and PLDs**
C.L. Westberg*, J. Vithayathil*, C.R. Coleman**, National Semiconductor Corp., Santa Clara, CA*, Futurenet Data I/O Corp., Chatsworth, CA**

10:25 **An Integrated Low-Cost Layout Toolbox for Custom IC Design**
D. Lucas, M. Chao, S. Srinivasan, IMP, San Jose, CA

10:50 **Symbolic Layout Synthesis for VLSI Design**
P.H. Hsieh, V. Chang, Chips & Technologies, Inc., Milpitas, CA

11:15 **SC2D: A Broad-Spectrum Automatic Layout System**
D.D. Hill, AT&T Bell Labs, Murray Hill, NJ

THURSDAY MORNING — Rose Room (Hilton)

QUICK-TURN GATE ARRAY APPROACHES

Chairman: M. Hollabaugh
Co-Chairman: C. Erdelyi

8:45 **A Second Generation User Programmable Gate Array**
H-C Hsieh, K. Duong, J.Y. Je, R. Kanazawa, L.T. Ngo, L.G. Tinkey, W.S. Carter, R.M. Freeman, Xilinx, San Jose, CA

9:10 **High Performance CMOS EPROM Programmable Bus Interface Controller**
K.S. Hallenbeck, R.W. Swartz, D.R. Pistone, Intel Corp., Folsom, CA

9:35 **High Density Laser Programmable Gate Array Family**
Z. Or-Bach*, K. Pierce**, S. Nance**, Efron Electronic Industries Ltd., Haifa, Israel*, VLSI Technology, Inc., San Jose, CA**

TECHNIQUES FOR DESIGN DATABASE MIGRATION

Chairman: S. Stevens
Co-Chairman: R. Jerdonek

10:00 **Electronic Design Interchange Format (TUTORIAL)**
A.R. Newton, Univ. of California, Berkeley, CA

10:50 **SCORE Cell Development Environment**
R.S. Kirk*, R.J. Hall**, R.H. Lathrop**, Gould Semiconductor Div., Santa Clara, CA*, MIT Artific Cambridge, MA**

11:15 **A Workstation Independent Approach to Building Performance-Optimized Gate Array Ma**
B. Hoffman, G. Barbera, Honeywell, Inc., Colorado Springs, CO

THURSDAY MORNING — Music Box Theatre

COMMUNICATION AND DATA PROCESSING CIRCUITS

Chairman: D.E. Brown
Co-Chairman: F. Yassa

8:45 **A Multi-Mode PCM Transceiver Chip for 1.544Mb/s Digital Telecommunications**
J.O. Kolczmeyer*, H.J. Canal*, E.H. Kisscon-Dunn*, R.D. Howson*, H. Park**, P. Alijafari** NJ*, AT&T Bell Labs. Allentown, PA**

9:10 **A Bit Serial Viterbi Decoder Chip for the MBit/s Range**
J. Stahl, H. Meyr, Aachen Univ. of Technology, Aachen, West Germany

9:35 **A 45 Mbit/Sec CMOS VLSI Digital Phase Aligner**
R.R. Cordell, Bell Communications Research, Red Bank, NJ

10:00 **A CMOS Processor for a 1000 Word Speech Recognition System**
W. Drews, R. Laroia, J. Pandel, A. Schumacher, A. Stoelzle, Siemens, Munich, W. Germany

10:25 **A Versatile Data String Search VLSI**
M. Hirata, H. Yamada, H. Nagai, K. Takahashi, NEC Corp., Kanagawa, Japan

10:50 **Double-Bit Error Correction Chip Set**
L. Peterson, S. Wang, L. Gal, Burroughs Corp., San Diego, CA

THURSDAY MORNING — Pavilion (Hilton)

MEASUREMENT AND RELIABILITY

Chairmen: T.M. Kelley
S.R. Quigley

8:45 **Pitfalls in Testing Digital ASIC Devices**
D.H. Armstrong, Hewlett-Packard Co., Boulder, CO

9:35 **On-Chip Propagation Delay Measurement**
D.J. Radack, L.W. Linholm, National Bureau of Standards, Gaithersburg, MD

10:00 **Military Qualification of Gate Arrays**
C.H. Windisch, Jr., Rome Air Development Center, Griffiss AFB, NY

10:25 **An ASIC Standard Evaluation Chip**
W.R. Huber*, D.R. Reganold*, P. Duncan**, General Electric, Research Triangle Park, NC*, Univ. of Florida, Gainesville, FL**

10:50 **A Static RAM as a Fault Model Evaluator**
J.M. Acken, M. Horowitz, Stanford University, Stanford, CA

11:15 **Metal Migration Considerations in Signal Lines**
J. Wright, C. Edmondson, Gould, Inc., Pocatello, ID

11:40 **Self-repairing Semiconductor Memory Chip with Improved Availability/Reliability**
O. Kowarik, Universitat der Bundeswehr, Neubiberg, West Germany

THURSDAY AFTERNOON — State Room (Hilton)

PHYSICAL OPTIMIZATION

Chairman: H-F. Stephen Law
Co-Chairman: R. Jerdonek

1:20 **A New Two-Dimensional Compaction Algorithm for Symbolic Layout**
J. Weinstein, Clarity, Ltd., Herzlia, Israel

1:45 **KCOMP: A Full Chip Compaction Strategy**
R.M. Kossey, AT&T Bell Labs, Murray Hill, NJ

2:10 **An Effective Hierarchical Approach to High Complexity Circuit Layout**
C-P Hsu, S. Evans, J. Tang, K. Chow, R. Perry, J. Liu, Hughes Aircraft Co., Newport Beach, CA

2:35 **An Improved Macrocell Placement Algorithm Using Simulated Annealing**
M-K Vai, M.A. Shanblatt, Michigan State Univ., East Lansing, MI

3:00 **GRIM: A Fast Simulated Annealing Program for Standard Cell Placement**
L.K. Grover, AT&T Bell Labs, Murray Hill, NJ

3:25 **A New Floorplan Representation for VLSI Design**
M-L Yu, AT&T Bell Labs, Holmdel, NJ

3:50 **A Gridless Switchbox Router**
R.B. Pyke, Seattle Silicon Corp., Bellevue, WA

THURSDAY AFTERNOON — Rose Room (Hilton)

ANALOG ARRAYS AND CIRCUIT TECHNIQUES

Chairman: D.A. Wayne
Co-Chairman: H.D. Barber

1:20 **A High Frequency Complementary-Bipolar Array for Fast, Analog Circuits**
B.W. McNeill, AT&T Bell Labs, Reading, PA

1:45 **"Standard Tiles": A New Design Method for High Performance Analog ICs**
P. Meza, W. Gross, Tektronix, Inc., Beaverton, OR

2:10 **A 6 GHz Analog Master Chip Utilizing SPICE as the Complete CAD Interface**
B. Fine, G. Heyes, VTC Inc., Bloomington, MN

2:35 **Nonlinear Analog Function Synthesis with MOS Technology**
J.W. Fattaruso, R.G. Meyer, Univ. of California, Berkeley, CA

3:00 **A Low Power Dissipation PLL IC Operating at 128MHz Clock**
K. Kato*, T. Sase*, H. Sato*, I. Ikushima**, S. Kajima***, Hitachi Res. Lab, Ibaraki, Japan*, Hitachi Optical Tech., Kanagawa, Japan**, Takasaki Works, Gunma, Japan***

3:25 **A Monolithic Bipolar Superheterodyne Receiver**
M.A. Krause, R.W. Brown, Siltronics Ltd., Kanata, Canada

3:50 **Noise Problems in Mixed Analog-Digital Integrated Circuits**
J.A. Olmstead, S. Vulih, RCA, Somerville, NJ

THURSDAY AFTERNOON — **Music Box Theatre**

PACKAGING AND INTERFACE APPLICATIONS

Chairman: D.M. Lewis
Co-Chairman: A.I. Lakatos

1:20 **Package and Board Level Modeling for VLSI Applications**
H.K. Charles, Jr., G.V. Clatterbaugh, The Johns Hopkins University, Laurel, MD

1:45 **Package Cracking Concerns in the Automated Handling of SMCs**
D.G. Mikan, Jr., J.S. Ferrario, IBM Corp., Poughkeepsie, NY

2:10 **Non-Custom IC with Custom Interface and Package**
L.D. Hobson, Burr-Brown Corp., Tucson, AZ

2:35 **A New Linear Line Driver/Receiver IC for Automotive Applications**
J.K. Monarty*, R.C. Jones**, T.L. Dinkledine*, Delco Electronics Corp., Kokomo, IN*, Texas Instruments Inc., Dallas, TX**

3:00 **A Radiation Powered Single Chip EEPROM ID Code Transceiver**
J.G. Nolan*, Z. Siemiatkowski**, Sierra Semiconductor, San Jose, CA*, Allen-Bradley, Santa Cruz, CA**

THURSDAY AFTERNOON — **Pavilion (Hilton)**

CONVERTER AND SENSOR CIRCUITS

Chairman: J.C. Tandon
Co-Chairman: A. Grebene

1:20 **A 12 Bit Gain-Ranging Data Acquisition System**
G. McGlinchey, Analog Devices, Palo Alto, CA

1:45 **A Pipelined Digital A/D Converter**
B. Guo, R. Gnansekaran, J. Kubinec, B. Johnson, Univ. of Nevada, Reno, NV

2:10 **A 160MHz Full-Flash Analog to Digital Converter**
M. Reyebi, J. Bondoc, N. Bhandari, Fairchild Semiconductor Res. Lab, Palo Alto, CA

2:35 **A CMOS Realization of Eight 32-Tap Transversal Filters on a Single Chip**
Y-S Lee, K.W. Martin, University of California, Los Angeles, CA

3:00 **Generalized Smart Sensor Array Electronics**
J. Trontelj*, L. Trontelj*, V. Kunc*, M. Stiglic*, G. Shenton**, M. Robinson***, G. Warren***, C. Jungo***, Univ. Edvard Kardelj, Trzaska, Yugoslavia*, IMP Europe, Swindon, England**, IMP, San Jose, CA***

3:25 **An Application Specific Integrated Circuit (ASIC) with CMOS-Compatible Light Sensors for an Optical Position Encoder**
P. Aubert, H. Oguey, Centre Suisse D'Electronique et de Microtechnique S.A., Neuchatel, Switzerland

3:50 **A Wide-Bandwidth, High Accuracy Logarithmic Amplifier for Line-Scan Imaging Systems**
M.J. Zuber, L.G. Moore, Jr., Eastman Kodak Co., Rochester, NY

4:15 **LATE PAPER**
"450 Megahertz DAC with Multiplexed Data Port"
D. Wilcox, S. Molin, Brooktree Corp., San Diego, CA