[招待論文]　Design-Manufacturing Interface for .13 um and below

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Extended Summary:

This talk will present the requirements for the design-manufacturing interface for the upcoming generations of ULSI technologies. We will start by presenting an overview of trends in semiconductor industry: accelerated roadmap which leads to further miniaturization, the increasing role of manufacturing fluctuations, shrinking time to market, product complexity (including SOC) and the overall disaggregation of semiconductor industry (emergence of fabless companies and increasing role of foundries in manufacturing). Then we will discuss the present, isolated approach to process development, product design and manufacturing. We will illustrate the current practices by several examples of state-of-the-art Design For Manufacturability (DFM) approaches showing both the EDA tools and databases.

We will then propose requirements for the integrated approach to DFM, which will include the following features:

- Process characterization (including characterization vehicles) to identify the key yield loss reasons (systematic, parametric, random defects)
- Abstraction of manufacturability/reliability design rules including sub-wavelength litho (OPC, PSM) and realistic worst-case files
- Cost modeling and forecasting.

These DFM interface capabilities will re-define the design flow and will pose new requirements on the EDA. They will enable much more *predictive design* synthesis and much more *realistic* verification of the system before its manufacturing. The next part of the talk will propose such a design flow utilizing this DFM interface. We will focus on the following:

- Technology choice (forecasting of performance, yield, cost and ramp-up)
- Constraint propagation to high-level synthesis system
- High-level design decisions using technology abstraction (monolithic vs. 2.5D, choice of IP cores, etc.)
- Estimation of timing, signal integrity, power statistical distributions
- Circuit design optimization for SOC - including mixed-signal components (design centering, timing optimization)
- Layout optimization (including model-based OPC).

We will conclude the talk by discussing the technical and organizational challenges that must be overcome to successfully implement the new design-manufacturing interface.

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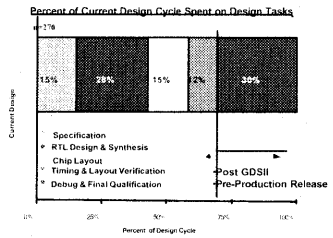
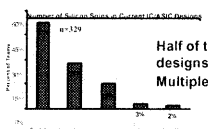
Distribution of Design Tasks



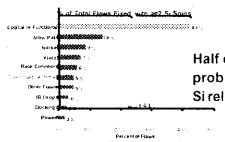
Lot's of Design Occurs after Tape-out

Re-spin Rate

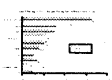


Half of the designs have Multiple spins

True across multiple industry sectors

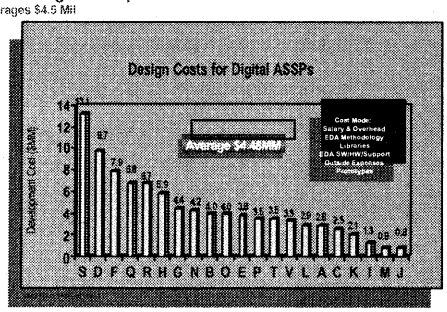


Half of the problems are Si related



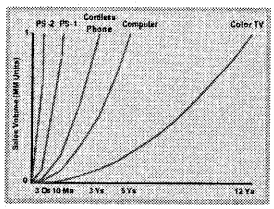
Escalating Development Cost

Averages $4.5 Mil



Time to volume is decreasing

Once in production there is little time to work things out



- Time to Volume (as defined as time to 1M units) is decreasing dramatically

Technology: New Processes

Deep-submicron technologies require new materials

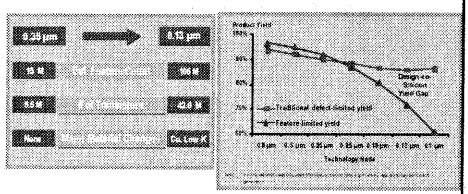
Process Module	150nm	180nm	130nm	90nm	65nm	45nm
Litho	248nm	248nm + OPC	248nm + OPC	193nm + OPC/PSM	193nm + OPC/PSM	157nm + OPC/PSM
Interconnect	Al-Cu	Al-Cu	Cu	Cu	Cu	Cu alloy
Interconnect Dielectric	TEOS	FSG	FSG	LowK	LowK	Porous LowK
Gate Electrode	Dual Poly	Dual Poly	Dual Poly	Dual Poly/ SiGe	Poly/ SiGe/Poly stack	SiGe/Metal
Gate Dielectric	SIO2	SIO2	SIO2	SIO2 SION	SIO/SIN stack HiK (for LV)	HiK
Salicide	Ti-Si	Co-Si	Co-Si	Co-Si	Ni/Co-Si	Ni-Si/Pt-Si
Substrate	P-Epi	P-Epi	P-Epi	Epi/SOI	SOI/Strained silicon-SiGe	SOI/Strained silicon-SiGe

- **Need twice the manufacturing efficiency with new materials as we achieved with old materials, for same yield**

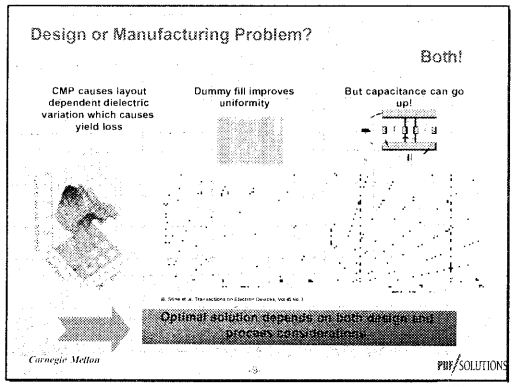
Problems

- Design marginality
  - ⇨ **IC design not robust enough, too sensitive to process fluctuations or environmental factors (supply voltage, temperature)**
- Process-related yield losses:
  - ⇨ **misprocessing (e.g., equipment-related)**
  - ⇨ **systematic effects**
  - ⇨ **random defects**
- Testing issues:
  - ⇨ **insufficient fault coverage in testing (test escapes)**
  - ⇨ **incomplete testing (does not fully represent IC operation in the field - e.g., simultaneous switching in the system not taken into account)**
  - ⇨ **test-related yield losses (incorrect testing)**
- Reliability:
  - ⇨ **transistors**
  - ⇨ **interconnect**

Technology: Escalating Complexity



- For every generation, we doubt complexity /cm^2 of area
- Manufacturing tolerances for features (e.g., contacts, vias, transistors) gets twice as tight as previous generation


Design or Manufacturing Problem?
Both!
CMP causes layout dependent dielectric variation which causes yield loss
Dummy fill improves uniformity
But capacitance can go up!
Optimal solution depends on both design and process considerations
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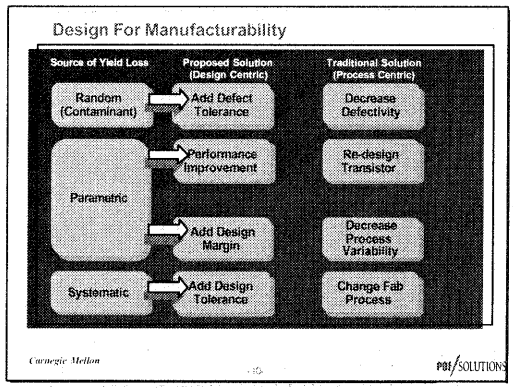
Design For Manufacturability
Source of Yield Loss
Proposed Solution (Design Centric)
Traditional Solution (Process Centric)
Random (Contaminant)
Add Defect Tolerance
Decrease Defectivity
Parametric
Performance Improvement
Re-design Transistor
Add Design Margin
Decrease Process Variability
Systematic
Add Design Tolerance
Change Fab Process
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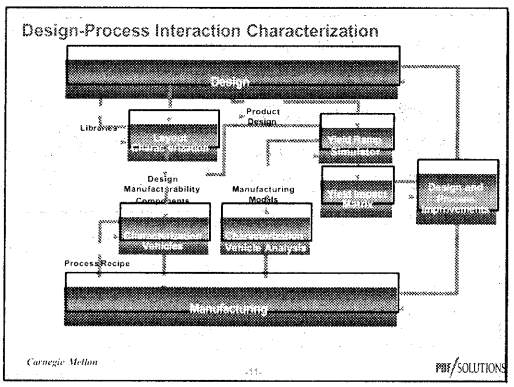
Design-Process Interaction Characterization
Design
Libraries
Product Design
Design Manufacturability Components
Manufacturing Models
Vehicles
Vehicle Analysis
Process Recipe
Manufacturing
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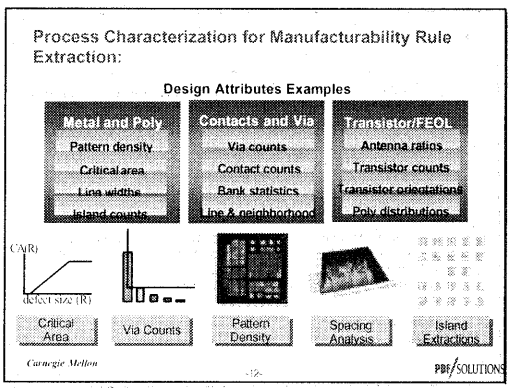
Process Characterization for Manufacturability Rule Extraction:
Design Attributes Examples
Metal and Poly
Pattern density
Critical area
Line widths
Island counts
Contacts and Via
Via counts
Contact counts
Bank statistics
Line & neighborhood
Transistor/FEOL
Antenna ratios
Transistor counts
Transistor orientations
Poly distributions
CA(R)
defect size (R)
Critical Area
Via Counts
Pattern Density
Spacing Analysis
Island Extractions
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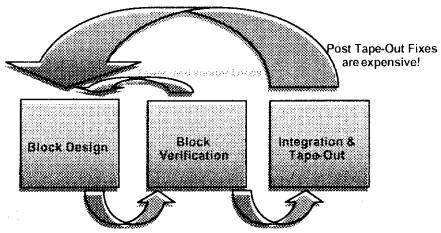
Catch problems earlier in the design cycle



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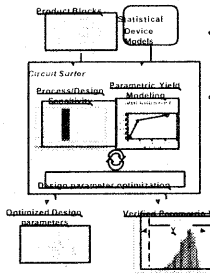
Parametric Yield Improvement Tool-Box



- Parametric Yield Verification
  - Response Surface Modeling (RSM) for accurate parametric yield estimation
- Design Optimization
  - Circuit Surfer maps process and design effects to circuit performances
  - Design or process parameter changes to optimize yield
  - Process window characterization

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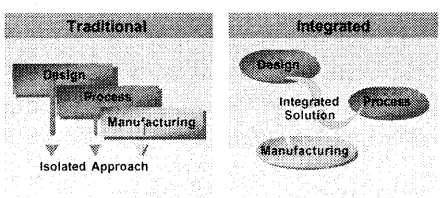
Integrated approach is required



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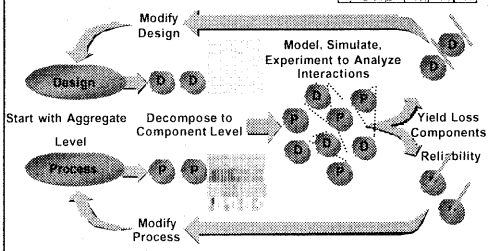
Integrated Approach



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