［特別招待論文］

SPARCハイエンドプロセサの設計手法

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Key concepts of design methodology

- Tight requirements
  - GHz processor design　1.3 GHz
  - Newest semiconductor process　130 nm
  - Short development schedule　14 months
- Key concepts of implemented design methodology
  - Hierarchical design & custom design
  - Rule-driven implementation
  - Timing-centric design flow
  - EC(Engineering Change)-base design

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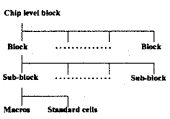
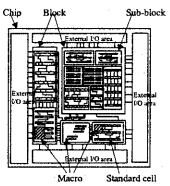
Hierarchical design & custom design

- 4-level hierarchical structure





- Custom design
  - Blocks and sub-blocks are hand crafted with assisted tools.
  - Standard-cell base macros are designed on-the-fly.

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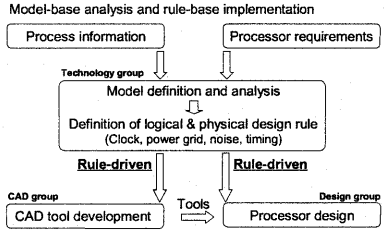
Rule-driven implementation

- Model-base analysis and rule-base implementation



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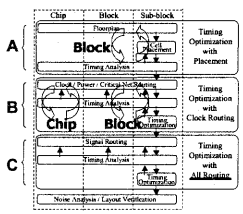
Timing-centric design flow

- Quick TAT in iteration
  - Timing optimization and analysis are continued daily in each block.
  - Timing in chip level is analyzed every few days.
  - Actual routing of non-critical signal nets for timing analysis is deferred as late as possible.



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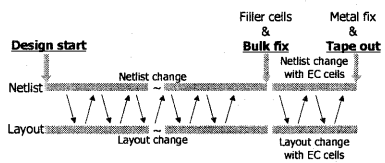
EC(Engineering Change)-base design

- Names of instance and net are preserved as much as possible.
- Timing is improved continuously with EC process.



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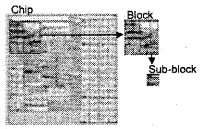
Floorplan

- Floorplan of Sparc64 microprocessor
  - Each sub-block may have transistor-base custom macros and cell-base custom macros besides standard cells.



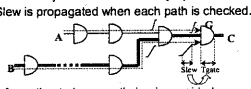
  - All blocks and sub-blocks are connected by abutment.
  - Global power and clock nets are routed in chip level.

Custom design and layout

- Transistor-base custom design
  - Flow and tools are the same as those for the cell design.
- Standard-cell base custom design
  - Flow and tools are the same as those for the chip design.
    - ✓ Chip designers can design on-the-fly.
    - ✓ Macros are not characterized.
    - ✓ Macros are expanded before timing analysis.
  - Productive P&R editor is one of keys to successful custom design.
    - ✓ Used to edit and view every data
    - ✓ Guides designers to lead error-free design
    - ✓ Links directly with other tools
      - Placer, router, timing analysis, DRC/LVS, ...

Timing analysis

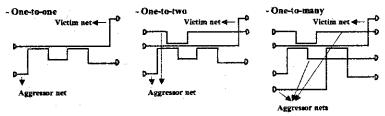
- Approach
  - STA algorithm is used.
  - False paths are specified by designers.
  - Latch and choppers can be used in the design.
  - Steiner-base capacitance extraction is available.
  - Clock delay can be measured by Spice.
  - Slew is propagated when each path is checked.



  - Information to improve timing is provided.
  - Utilities to analyze paths are available.
    - ✓ Slack calculation, path trace, etc.

Noise analysis

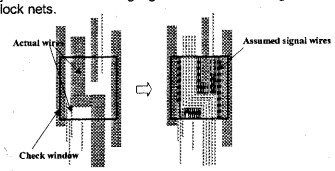
- All possible combinations are checked.
- Three types of combination are checked.



- Timing window and slack are considered for one-to-two check.
- Analysis is performed hierarchically.
- Some of error nets are modified by a spacing router.

Design for manufacturability

- Metal density is checked assuming signal wires after routing of power and clock nets.



- Single vias are replaced by double vias as many as possible.
- Spacing router is applied.

Summary

- Methodology is successfully applied to SPARC64 microprocessor design.
  - Schedule: 14 months (from start to implementation)
  - Performance: 1.35GHz in production
- Hierarchical design and custom design are used.
  - Custom macros (transistor-base and cell-base)
  - Custom blocks and sub-blocks
- Performance is continuously improved by EC-base design.
- Rule-driven implementation shortens the TAT of analyses.
  - Power grid
  - Clock distribution circuit