社団法人　情報処理学会　研究報告
IPSJ SIG Technical Reports

2005－ＳＬＤＭ－121（14）
2005／10／20

[招待論文]心理学的脳モデルVLSIシステムを用いた柔軟な画像認識

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あらまし チップ上に過去の記憶を大量に備え、入力事象にもっともよく似た過去の事例を瞬時に連想想起することで柔軟な判断を実行する、心理学的脳モデル VLSI システムを開発した。このシステムを用いてロバストな画像認識が行えるよう、64×64 ピクセルのグレースケール画像を 64 次元の特徴ベクトルとして表現する、新たなベクトル化アルゴリズムを開発した。これは、入力画像より方向性エッジを抽出し、その空間ヒストグラムによって画像をベクトル表現する一種の画像の圧縮手法である。人間の目によく似通って見えるものは、ベクトル空間においても近い位置にマッピングされるという優れた特性を持つ。手書きパターン認識、医用X線写真解析、顔検出等への応用例で、大変ロバストな特性が実証された。このベクトル生成は、非常に計算コストの高いものであるが、専用チップの開発により、100MHz の動作で、2.2GHz プロセッサ搭載の PC 上のソフトウェア処理と比較して、約一万倍の高速化を達成した。

キーワード VLSI, アナログ VLSI, デジタルプロセッサ, 画像処理, 画像認識, ベクトル量子化

A Psychologically-Inspired VLSI Brain Model System for Human-Like Image Recognition

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Abstract A psychologically-inspired VLSI brain model has been developed to perform human-like flexible information processing. The system stores a vast quantity of past experience in the on-chip memory and the most relevant event in the past is automatically recalled in an immediate response to the current input. Since the search is carried out by a fully parallel processing on the chip, the response is extremely fast. In order to carry out human-like image recognition using the system, an edge-based image representation algorithm called Projected Principal-Edge Distribution (PPED) has been developed. It represents a two-dimensional image by a feature vector that very well preserves the human perception of similarity of images in the vector space, thus allowing us to perform robust image classification. The application of the system to handwritten pattern recognition, medical radiograph analysis, and face detection are presented as illustrative examples. Since the PPED vector generation is a computationally very expensive processing, a dedicated vector-generation VLSI processor employing mixed-signal architecture has been developed aiming at real time applications.

Keyword VLSI, analog VLSI, digital processor, image processing, image recognition, vector quantization, psychological brain model, soft computing

1. Introduction

Despite the ever-increasing performance of computers, human-like flexible information processing is not quite possible yet. In our daily life, we solve most of the problems largely relying upon our experiences in the past. Specialists also carry out their professional jobs based on their expertise knowledge accumulated through their long experience and discipline. In either case, association and intuition based on the memory of the past experience play an essential role [1-3]. The scheme is very different from that in digital computers. Computers solve problems by sequential logic and numerical processing, the procedure being prescribed as software programs specifically tuned to individual problems. On the other hand, medical doctors, for instance, make diagnoses by fully utilizing their professional experience. It seems almost impossible to fully describe the judgment process carried out in their minds as computer programs.

In this article, we propose a new electronic computing system that finds solutions not by numerical computation but by association to the experience in the past [4]. We have been developing VLSI systems, mimicking the mind processing at

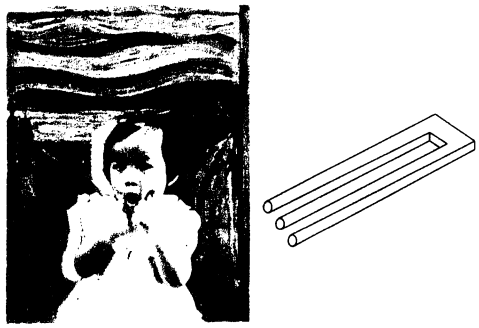


Fig. 1. The background scenery of the picture on the left reminds us of Munch's "Scream". But in the next moment, we notice the strange person is replaced by a cute girl. The recalling of Munch's drawing is an unconscious automatic processing in the brain. Similar automatic recalling prevents us from understanding the topology of the drawing on the right. Such observation has led us to develop a VLSI hardware specific to automatic recalling of past experience: the associative processor.

the very hardware level [5, 6]. Namely, the association is carried out not by software but by elementary circuits and devices directly. Although the research is still in the developmental stage, some preliminary experimental results are presented as promising examples. They include the applications to handwritten pattern recognition [7], medical radiograph analysis [8], and face detection [9]. The organization of this article is as follows. In Section II, the human-intelligence system based on the psychologically-inspired VLSI brain model is presented. VLSI implementation of associative processors, the key element in the system, is presented in Section III. Image vector generation algorithm and the results of image recognition experiments are presented in Section IV. VLSI chips for early visual processing including the vector generation VLSI are described in Section V and the conclusions are given in Section VI.

2. A Human-Intelligence System Based on Psychologically-Inspired VLSI Brain Model

What do we think when we look at a drawing like that in Fig. 1? We will be puzzled. From the background scenery, we recall "Scream" of Munch. But in the next moment, we notice the strange person is replaced by a cute girl. The recalling of Munch's drawing is not the result of logical thinking but a conclusion drawn by an unconscious automatic processing in the brain. A VLSI processor dedicated to such automatic recalling processing is called *associative processor*, a hardware analogue to the columnar architecture in the neocortex of the brain. The associative processor architecture is described as a maximum-likelihood search engine having a fully-parallel search capability using on-chip huge database memories.

Fig. 2 illustrates the total view of the VLSI human-intelligence system we are developing [4] in which the associative processor plays a key role. Both analog [6, 10] and digital [5] chips have been developed for associative processor implementation. An analog associative processor employing ferroelectric memory for template vector storage has also been developed [11].

The saliency detector chip is utilized to detect the region of interest (ROI) for selective attention. This particular chip was designed to detect the ROI based on the objects' motion. Namely, the object having the largest movement in the scene is detected. The chip can detect multiple moving objects in a cluttered background scenery using the quasi two-dimensional focal plane processing [12-14]. Stereo vision chip is utilized for range measurement to provide auxiliary information in scene analysis. When an ROI is detected, the 64 x 64-pixel image (the elementary recognition kernel in our system) is converted to a 64-dimension feature vector so that the associative processor can perform image perception [8]. The image-to-vector conversion is computationally very expensive and several VLSI chips have been developed based on analog [15], digital [16] and mixed signal [17] architectures.

3. VLSI Implementation of Associative Processors

An associative processor is a maximum-likelihood search engine having a fully-parallel search capability using the on-chip huge database memory. Associative processor chips have been implemented in both CMOS digital [5] and analog technologies [6, 10]. Digital implementation features high flexibility in associative processing with various options, while analog implementation offers compact and low-power features.

The chip photomicrograph in Fig. 3 is an example of digital implementation [5]. It features a very fast winner search employing a two-dimensional bit propagating WTA (Winner-Take-All) circuitry. Flexible template configuration has been achieved by introducing a new variable binary-block addressing scheme. Both Manhattan and Euclid distances with weight multiplication to each element are made available with a minimal area penalty. Use of such versatile features of digital associative processors in intelligent internet search applications is described in Ref. [18].

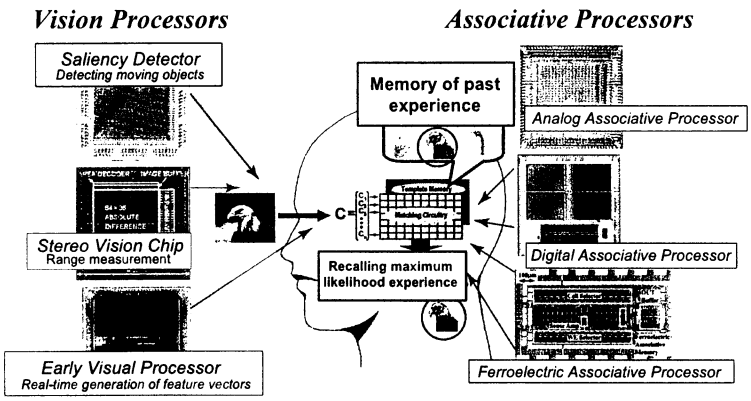


Fig. 2. System organization of VLSI human-intelligence system. The region of interest is detected based on the objects' motion and its image is transformed to a vector (a reduced representation). Then the maximum-likelihood image in the memory storing past experience is automatically recalled by the associative processor, a hardware analogue to the columnar architecture in the neocortex of the brain.

Fig. 4 schematically illustrates the architecture of the two-dimensional bit propagating WTA. A tournament is carried out to locate the winner (the smallest distance input) among the N input values. This requires log N tournament stages. At each stage, comparisons are made for all pairs simultaneously. Usually a word comparator is used for comparison of a pair of m-bit numbers, which produces a delay time on the order of log m at each stage if a carry look-ahead adder is used as a word comparator. As a result, the total delay time would be on the order of log m x log N. In the two-dimensional bit propagating architecture, on the other hand, bit comparators are used instead of word comparators. The bit comparison is started from the MSB of all numbers and the result is immediately transmitted to the next stage bit comparator in the tournament tree as well as to the second MSB in the same-stage bit comparators. As a result, the total delay time becomes on the order of m + log N. This is definitely faster than the delay of log m x log N since N is usually a large number. The measurement results from the fabricated chip are shown in Fig. 5.

In analog implementation, on the other hand, vast-scale integration under low power operation is possible, providing the opportunity for use in mobile applications where memory and computational resources are severely limited. Fig. 6 shows examples of element matching circuits between an input vector and a memorized template vector [6]. The circuits utilize the bell-shaped current-voltage characteristics of the CMOS-inverter shortcut current [19]. The preprogrammed peak position represents the template value and the current yields the similarity measure between the template and the input. By introducing the concept of the neuron MOS [20] (or floating-gate MOS), the

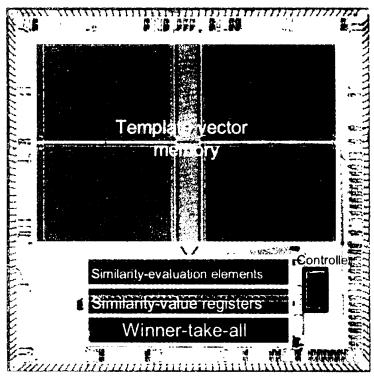


Fig. 3. General purpose associative processor implemented in a 0.6μm-CMOS double-poly technology.

functional forms in the similarity evaluation were made real-time tunable as shown in Fig. 7.

The vector matching circuit that evaluates the similarity between the input and the template vectors is easily composed by taking the wired sum of all I_{OUT}'s from element matching circuits as shown in Fig. 8. I_{SUM}, the sum of I_{OUT}'s, is then sunk through the NMOS receiving V_{RAMP} at its gate. This forms a current comparator circuit for I_{SUM} and the sink current in the NMOS. Then the identification of the maximum-likelihood template vector is very easily carried out by just giving a common ramp voltage to the V_{RAMP} nodes of all the vector matching circuits. When V_{RAMP} is ramped down from V_{DD} to 0V, the vector matching circuit yielding the maximum I_{SUM} firstly upsets and its output voltage (V_{OUT}) shows a 0-to-1 transition. Then the time domain WTA circuitry [21] is

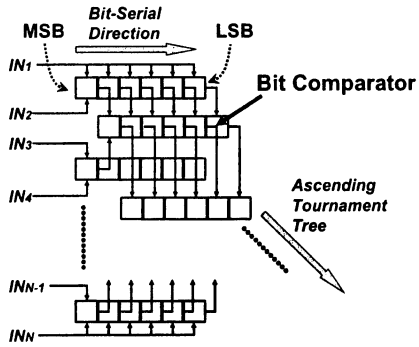


Fig. 4. Two-dimensional bit propagating WTA architecture. Total delay is proportional to log N + m (bit length) in contrast to log N x log m of word-comparator implementation.

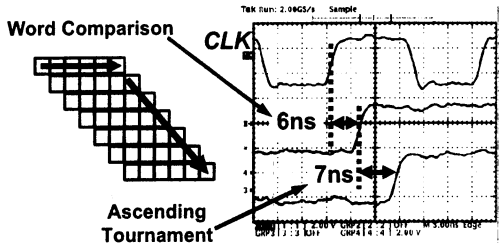


Fig. 5. Measurement results of winner search. Winner search is completed in 13ns for 6b 128 input vectors.

utilized to locate the winner. Fig. 9 shows a photomicrograph of the test chip of the analog associative processor.

The measurement results from the analog associative processor are demonstrated in Fig. 10 where the chip was used to identify a specific anatomical landmark on medical X-ray head films (cephalometric landmark identification). Template matching was carried out using the PPED vector representation [8] of X-ray images. The Sella (a pituitary gland) search experiments were conducted both in the above-threshold and sub-threshold regimes. The selection of operation regimes was done by changing the bias voltage V_{GG} in Fig. 6. The Sella pattern is delineated by a solid line on each figure. In the Sella search, the approximate center of the characteristic semi-circle pattern needs be identified. Correct positions are successfully detected as current peaks in both above-threshold (b) and sub-threshold (c) operation regimes. By operating the circuit in the sub-threshold regime, a very low-power operation of the system is possible. In the present experiment, no degradation in position detection accuracy was observed when the operation current was reduced by three orders of magnitude by reducing the V_{GG} bias. Since the pattern matching algorithm using the PPED representation is very robust against small variations in the vector element operations, the analog associative-processor-based image recognition would be a very promising approach toward future low-power intelligent systems, in particular, in mobile applications.

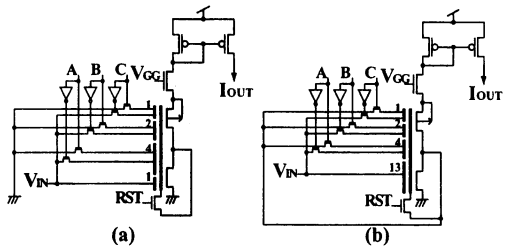


Fig. 6. Schematic of vector-element matching circuits: (a) Gaussian type; (b) plateau type.

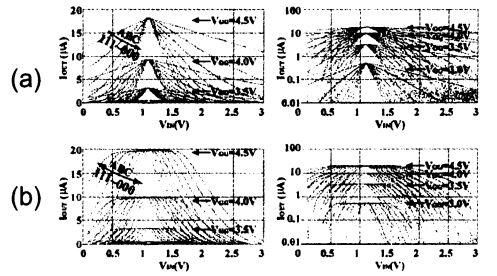


Fig. 7. Measured characteristics of element matching circuits: (a) Gaussian type; (b) plateau type. Circuits operate in the subthreshold regime when V_{GG} is reduced, thus allowing us to perform very low power hardware computation.

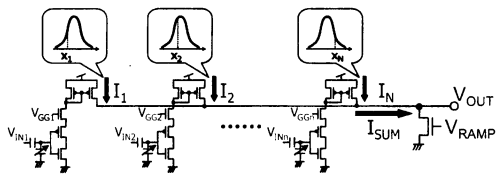


Fig. 8. Schematic of 16-dimension vector matching circuit.

Fig. 11 shows the separation of overlapping patterns conducted using the analog associative processor [6]. The circuit successfully separated the circle and the square in the first example (top), while it failed in the second example (bottom) where a triangle was erroneously detected. However, this error is not against our perception. In this regard, the circuit behavior is similar to ours even when making mistakes.

Fig. 9. Photomicrograph of the test chip of analog associative processor.

4. Feature Vector Representation of Images

Since an image contains massive quantity of redundant data, they must be compressed to form a feature vector. A feature vector must preserve the most essential features in the original image while achieving substantial dimensionality reduction. Of particular importance is that the representation must preserve the human perception of similarity among images. Namely, images similar to our eyes need be mapped closer in the feature vector space. For this purpose we have developed a "Projected Principal-Edge Distribution (PPED)" algorithm [8].

Fig. 12 illustrates the PPED vector generation procedure. The input image (64x64 pixels) is firstly subjected to pixel-by-pixel spatial filtering operations to detect edges in four directions: horizontal (HR); vertical (VR); +45 degrees (+45); and −45 degrees (-45). We used a 5x5 filtering kernel for each direction edge. Only one direction edge is assigned at each location provided its convolution result exceeds the threshold for edge detection at that location. The threshold is determined as the median value of all 20 luminance difference values between two neighboring pixels within the 5x5 kernel block. This thresholding is particularly important in extracting essential features from delicate gray scale images. The procedure is equivalent to the automatic gain control being carried out in the retina of our eyes.

Detected edges are represented by binary flags and four feature maps are generated for horizontal, +45-degree, vertical and −45-degree edges. We have treated the four feature maps as the most fundamental representation of the original image. The two-dimensional bit array in the feature map is further reduced to a one-dimensional array of numbers, i.e., a vector. In the PPED representation, this is done by projecting bit flags onto respective axis. Namely, the horizontal edge flags in every four rows are accumulated and projected onto vertical axis, thus generating an edge distribution histogram having 16 elements. The vertical, +45-degree and −45-degree edge flags are simi-

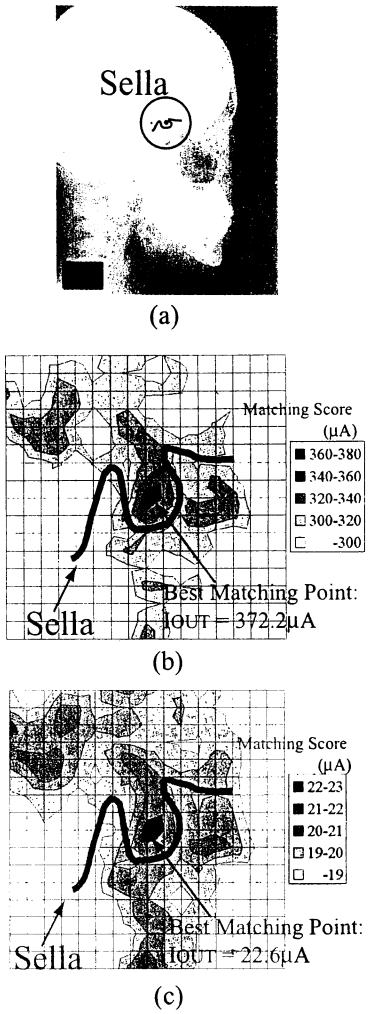


Fig. 10. Matching results of Sella search using Gaussian-type circuits: input image (a); current contour maps in above-threshold operation (b) and subthreshold operation (c).

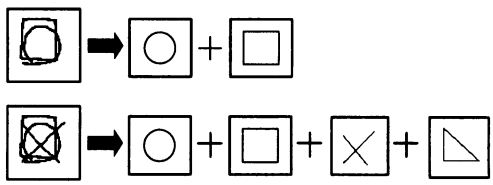


Fig. 11. Separation of overlapping handwritten patterns. False detection of a triangle in the triply overlapping patterns at the bottom is not against our perception.

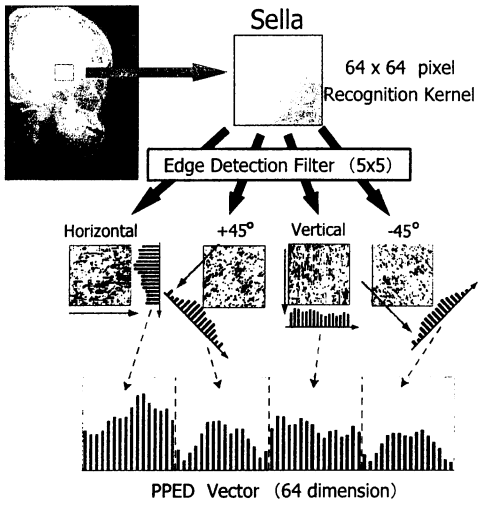


Fig. 12. PPED vector generation algorithm.

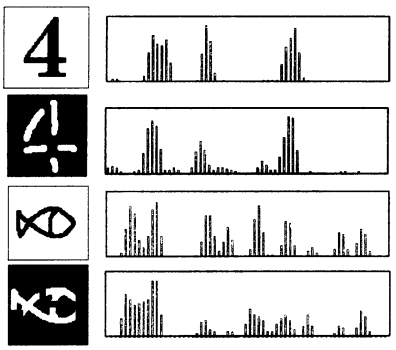


Fig. 13. Examples of PPED vectors. Human perception of similarity is well preserved in the vector representation.

larly projected onto horizontal, -45-degree and +45-degree axes, respectively. In this manner, four edge distribution histograms each having 16 elements are generated, and the four histograms are concatenated in the order of HR, +45, VR, -45 to form a 64-dimension feature vector. In this regard, we call the algorithm "Projected Principal-Edge Distribution (PPED)". The PPED vectors very well preserve the human perception of similarity among original images as shown in Fig. 13, thus enabling image classification by a simple template matching using associative processors. Detailed description of the PPED algorithm is given in Ref. [8]. Other forms of feature vectors generated from the four edge feature maps are proposed to make the recognition performance more robust [9]. Image recognition experiments using PPED representation have been conducted extensively by computer simulation in order to optimize the algorithm for

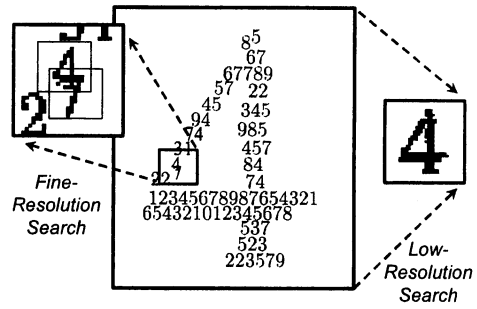


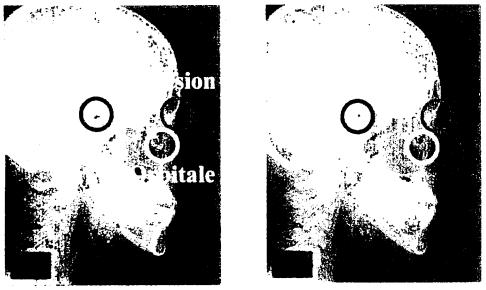
Fig. 14. Solving zoom lens metaphor problem by multi-resolution search.

hardware implementation. Some examples are presented in the following.

Fig. 14 illustrates the application to the so-called zoom lens metaphor problem. By introducing the concept of multi-resolution search, we solved the problem. The two overlapping digits "4" and "7" are successfully separated by the fine-resolution search. In the low-resolution search, on the other hand, the large image of "4" composed of small digits has been also correctly recognized [22]. General procedure for separating more complicated handwritten patterns using an analog associative processor chip is experimentally demonstrated in Ref. [6].

Application to grayscale image recognition is presented in the following. The PPED image representation was applied to cephalometric landmark identification (Sella, Nasion, and Orbitale) [8]. This is one of the most important practices of dentists in orthodontics, and automatic identification by computers was studied [23, 24]. The results are demonstrated in Fig. 15 where the recognition results by our system are compared with the results by three expert dentists having more than 10 years of experience in the university hospital. Very promising results are obtained.

Fig. 16 demonstrates a failure example. Totally different point is identified as Sella by our system in the picture on the left. However, the correct location is also identified as the minimum of the dissimilarity measure in the region including the real Sella pattern. But the false position was identified because it has a smaller dissimilarity measure due to an accidental match. In our perception, such an error would not happen because we would utilize more information taken from surrounding areas. Then, an analogous processing was tried in our system. Namely, the search was carried out by reducing the pixel resolution of both the target image and the template image. The low resolution search shown in the figure was carried out using the template size twice as large as that used in the



By Our System By Three Expert Dentists

Fig. 15. Results of cepholometric landmark identification experiment for Sella, Nasion, and Orbitale: by our system (left); by three expert dentists. (right).

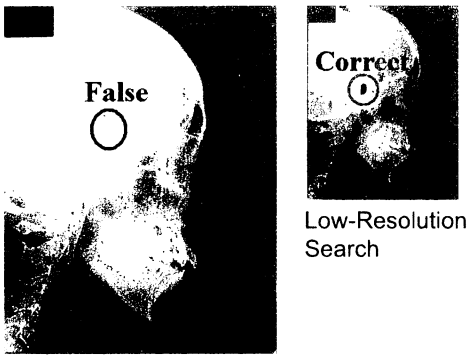


Fig. 16. False point is identified in the fine-resolution search using small-area templates (left), while the correct area is identified in the low-resolution search using templates of four times larger area (right).

fine-resolution search. (Four neighboring pixel data were averaged to one to reduce the resolution.) Since more surrounding information is included in the search, the correct area is detected. Then more precise localization was conducted by performing a fine-resolution search in the area specified by the low-resolution search.

Application to face detection [9] is presented in Fig. 17. Here the faces of 20 faculty members of EE department of The University of Tokyo were taken as face examples and search was carried out in a group photo of people [25] in which the human race, the image resolution and the exposure conditions are different. As shown in the figure, almost all faces are correctly detected. The false positive indicated in the figure looks like a human face to our eyes. Using the same template set, face detection was carried out for a realistic drawing as well as for an animal face.

The image recognition examples presented here

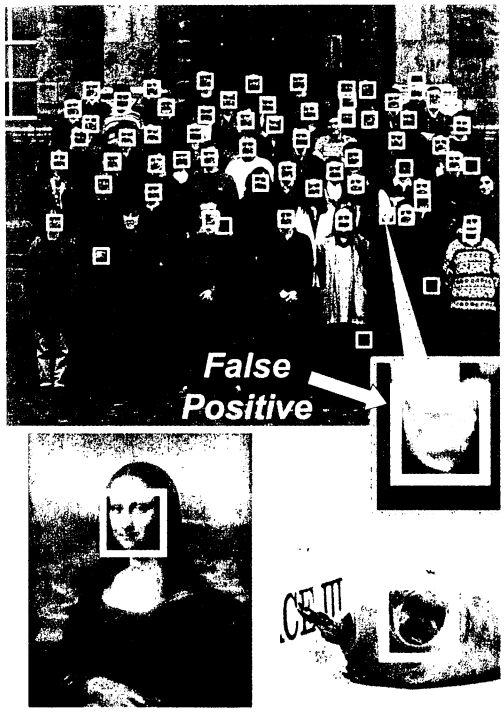


Fig. 17. Face detection results. Face samples were taken from frontal view of 20 Japanese people in a group photo (not shown here), and 2,000 non face samples were randomly taken from the background scenery of the photo.

are very different in nature from each other. It should be noted, however, that the algorithm is basically the same for all these examples and no specific tuning was introduced in each problem. In face detection algorithm, however, we have introduced two new vector representations generated from the same feature maps used in the PEDD vector generation and more careful decision process has been introduced based on the concept of multiple clue matching [9]. This allows us to perform more robust face detection [26].

5. VLSI Chips for Early Visual Processing

The most time consuming part in the recognition processing using associative processors is the PPED vector generation. Edge filtering operation using the local threshold determined from the median of local luminance variation distribution is computationally very expensive because the processing must be repeated pixel by pixel to scan across the entire image. For this reason, we have been developing various image processing VLSI chips in both digital [16] and analog [15] architectures. A mixed-signal image filtering VLSI has been developed aiming at real-time generation of

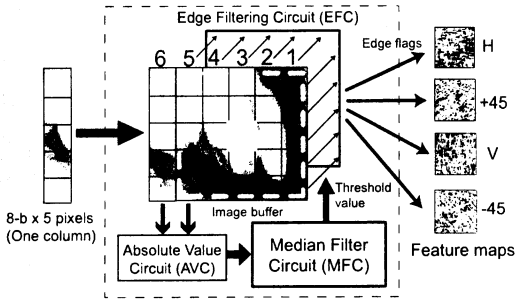


Fig. 18. System organization of feature map generator in PPED vector generation VLSI.

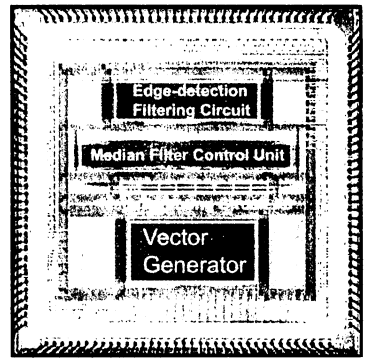


Fig. 19. Photomicrograph of PPED vector generation VLSI fabricated in a 0.35-μm double-poly triple-metal CMOS technology. Die size: 4.5mm x 4.5mm, power supply: 3.3V, operation frequency: 50MHz.

PPED vectors [17].

The circuit organization for the feature map generation is shown in Fig. 18. A four-stage asynchronous median detection architecture based on analog digital mixed-signal circuits has been introduced to determine the threshold value of edge detection, the key processing parameter in the vector generation. In order to achieve area efficient implementation, CMOS analog majority voting circuits were utilized for median detection. As a result, a fully seamless pipeline processing from threshold detection to edge feature map generation has been established. A prototype chip was designed in a 0.35-μm double-polysilicon three-metal-layer CMOS technology and the concept was verified by the fabricated chip shown in Fig. 19. The chip generates a 64-dimension feature vector from a 64x64-pixel gray scale image every 80μsec at a clock rate of 50MHz. The new version chip recently developed [27] generates a PPED vector every 0.6μsec at 100MHz of operation. This is about 10,000 times faster than the software processing on PC with a 2.2GHz processor, making a real-time image recognition system feasible.

6. Conclusion

A human-like intelligent VLSI system based on a psychologically-inspired architecture has been presented. The building block VLSI chips have been developed in both analog and digital CMOS technologies. A hardware-friendly image representation algorithm has also been developed and its robust nature in image recognition has been experimentally demonstrated. The system will play an important role in building real-time responding systems that would not be accessible with conventional digital computer systems because of the time and power constraints. Our system works like our right brains, i.e., the chip recognizes objects, not by sequential logic operations, but more intuitively by association to the experience in the past. Since the association is carried out by a fully-parallel computation on the chip, the response is very fast. If such a powerful associative function is combined with the logic processing capability of current microprocessor chips, human-like intelligent systems would be materialized. This is somehow analogous to the collaboration of the logic-intensive left hemisphere and the intuition-driven right hemisphere in our brains. If the expertise knowledge and experience of doctors, for instance, were embedded in the system, a very robust automatic diagnosis system implementation would become possible in future.

Acknowledgement

The authors are greatly indebted to Professor Kenji Takada, Department of Orthodontics, Faculty of Dentistry, Osaka University, Osaka, Japan for providing us his expertise knowledge in orthodontics and his collaboration in the research. The test chips in this study were fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), The University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

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