A Broadside Test Generation Method for Transition Faults in Partial Scan Circuits

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Abstract This paper presents a broadside test generation method for transition faults in partial scan circuits. In order to generate broadside transition tests for a given partial scan circuit whose kernel circuit is acyclic, this method transforms the kernel circuit into some combinational circuits called broadside test generation models. These models are constructed by using a time-expansion model of the kernel circuit. All the broadside transition tests are generated by performing constrained stuck-at test generation on the broadside test generation models. This method is effective in terms of over-testing as well as area overhead compared with enhanced scan testing and broadside testing based on full scan technique. Experimental results show that the proposed method can alleviate the over-testing issue in reasonable test generation time.

Key words transition fault, broadside test, broadside test generation model, constrained stuck-at test generation, over-testing

1. Introduction

Scan design is widely accepted by industry as an effective design for testability (DFT) method for delay faults as well as stuck-at faults. There is an essential difference between scan testing for stuck-at faults and that for delay faults. Unlike stuck-at testing, an additional consideration must be taken into account for delay testing using scan methodology. That is, to detect a delay fault, two consecutive vectors are needed to be applied to the faulty site in a scan environment. This can be done by using enhanced scan technique [1] or standard scan technique such as *skewed-load testing* [2] and *broadside testing* [3].

In [1], all the flip-flops (FFs) in a given circuit are replaced with enhanced scan FFs (ESFFs). Since each ESFF can store any two consecutive vectors, any two-pattern tests for delay faults in the circuit can be applied. However, the extra area and delay induced by ESFFs are very large. Moreover, over-testing, which is one of the main concerns during testing [4], [5], can happen. This issue is mainly caused by the detection of sequentially untestable faults. In a fully enhanced scan circuit, many sequentially untestable faults can unintentionally be detected because two consecutive vectors that are never applied during normal operation are settable to ESFFs. One way to handle this over-testing in delay testing is to adopt partially enhanced scan technique [6]–[9]. In a partially enhanced scan circuit, only some FFs are replaced by ESFFs. In other words, some FFs remain normal FFs. This means that sequentially untestable faults associated with the normal FFs are not made detectable. Thus, partially enhanced scan technique can reduce over-testing. However, this technique still requires special scan FFs (i.e., ESFFs).

In standard scan technique, standard scan FFs (hereafter simply referred to as scan FFs (SFFs)) are used instead of ESFFs. Since SFFs can store only an arbitrary vector, unlike ESFFs, the second vectors of two-pattern tests must be justified by using some technique. To achieve this, skewed-load testing and broadside testing have been proposed for full scan circuits. In skewed-load testing, the second vectors of two-pattern tests are derived by shift operation. This forces the scan signal to be operated at the rated speed, and the scan chain must be designed judiciously. Moreover, not only over-testing but also under-testing, in which testable faults are missed, can happen in skewed-load testing. Indeed, unnecessary (resp. necessary) two-pattern tests for a given circuit may (resp. may not) be shifted because applicable two-pattern tests depend on the order of SFFs on the scan chain. Broadside testing, in contrast, never causes under-testing. This is because the second vectors of two-pattern tests are derived by normal operation. Therefore, broadside testing is more desirable than skewed-load testing although broadside testing can also cause over-testing. There are several broadside test generation methods for full scan circuits [10]–[15]. In terms of area overhead and over-testing, partial scan design is an alternative solution. In [16], a transition test generation method

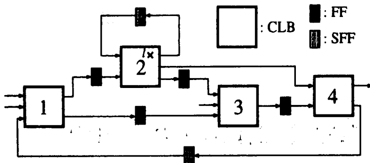

Figure 1: Partial scan circuit: S

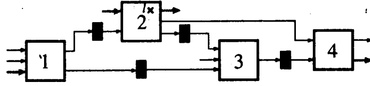

Figure 2: Kernel circuit of S: S_K

for partial scan circuits has been proposed. This method is based on skewed-load testing. As mentioned previously, since skewed-load testing has some undesirable properties, a test generation method based on broadside-testing is also needed for partial scan circuits.

In this paper, we propose a method of broadside test generation for transition faults in partial scan circuits. This method targets partial scan circuits whose *kernel* circuits are acyclic. To generate broadside transition tests for a partial scan circuit, we transform its kernel circuit into some combinational circuits. This transformed circuits, which are called *broadside test generation models*, are constructed by using a *time-expansion model* [17] of the kernel circuit. All the broadside transition tests are generated by performing constrained stuck-at test generation on the broadside test generation models. Compared with broadside testing based on full scan technique, this method is effective in terms of not only area overhead but also over-testing, i.e., the number of sequentially untestable faults unintentionally detected by the method is small. Through experiments, we show that out method can reduce over-testing in reasonable test generation time.

2. Related Works and Motivation

First, this section describes our target circuits and faults. Then, we explain some related works which motivate us to address this work.

2.1 Target Circuits and Faults

This paper targets partial scan circuits whose kernel circuits are acyclic. A sequential circuit can be represented as combinational logic blocks (CLBs) connected with each other directly or through FFs. A CLB is a region of connected combinational logic gates. Figure 1 is an example of a partial scan circuit S, and its kernel circuit S_K is shown in Figure 2. The input (resp. output) of an SFF in Figure 1 is treated as a primary output (PO) (resp. primary input (PI)) in Figure 2, which is represented as a bold arrow and called a pseudo primary output (PPO) (resp. pseudo primary input (PPI)). Note that, our method is still applicable to a full scan circuit with multiple scan chains. This is because, by enabling a subset of scan

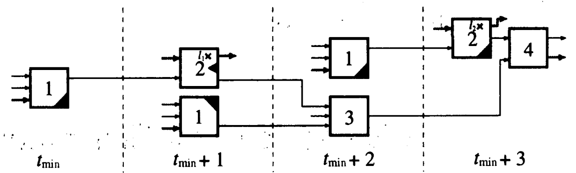

Figure 3: Time-expansion model of S_K: $C^T(S_K)$

chains such that the kernel circuit is made acyclic and treating SFFs on the other chains as normal FFs, we can apply our method to the kernel circuit. We handle a broadside test generation problem for *transition faults* in a partial scan circuit. There are two transition faults associated with each line in a circuit: a *slow-to-rise fault* and a *slow-to-fall fault*. It is assumed that, under the transition fault model, the extra delay caused by a transition fault is large enough to prevent the transition through the faulty site from reaching any FF or any PO within a specified period. In this paper, we assume that transition faults in a partial scan circuit are tested in the slow-fast-slow testing manner [18]. Under this assumption, we can consider a sequential circuit to be delay fault-free in both the fault initialization and fault effect propagation phases. Note that if a transition fault is testable under the at-speed testing manner, the fault is also testable under the slow-fast-slow testing manner [18]. Hence, slow-fast-slow testing never misses any fault testable in at-speed testing.

2.2 Double Time-Expansion Model

A *double time-expansion model* [9] has been proposed to generate transition tests for an acyclic sequential circuit. Given an acyclic sequential circuit, a double time-expansion model of the circuit is constructed from a *time-expansion model (TEM)* [17] of the circuit. In the following paragraphs, we briefly explain those two models.

A TEM of an acyclic sequential circuit is a combinational circuit in which the behavior of the circuit within a specific time span is simulated. Figure 3 is a TEM $C^T(S_K)$ of the kernel circuit S_K shown in Figure 2. TEM $C^T(S_K)$ is a combinational circuit derived by connecting CLBs according to their sequential depths. A sequential depth between two CLBs is defined as the number of FFs on a path between the CLBs. If a CLB has paths to another CLB in S_K whose sequential depths are different, the CLB is duplicated in $C^T(S_K)$. For example, in Figure 2, since CLB 2 has two paths to CLB 4 whose sequential depths (zero and two) are different, CLB 2 is duplicated in $C^T(S_K)$. A shaded part of a CLB in Figure 3 represents a portion of the lines and gates removed. There is no path from the portion to any input of CLBs or any PO and PPO of $C^T(S_K)$. The character placed at the bottom of each frame in Figure 3 is the label of CLBs in the frame, where t_{min} denotes an arbitrary integer. The label of a CLB v is denoted as $t(v)$ which corresponds to a specific time.

A double time-expansion model is defined as follows [9].

[Definition 1] Let S be an acyclic sequential circuit, and $C^T(S)$ be a

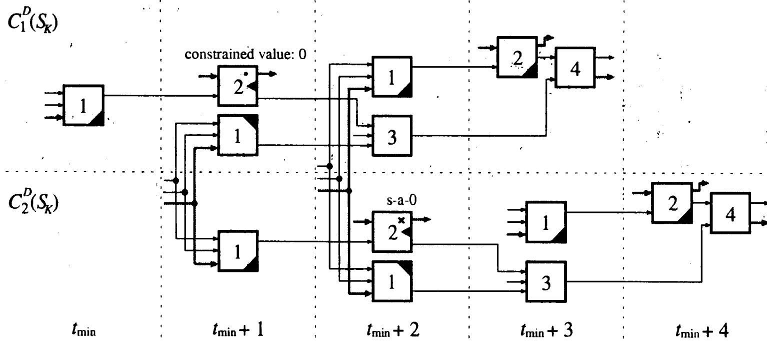

Figure 4: Double time-expansion model of S: $C^D(S_K)$

TEM of S. Then, a combinational circuit obtained by the following procedure is said to be a double time-expansion model (DTEM) $C^D(S)$ of S.

S1: Make two copies of $C^T(S)$: $C_1^D(S)$, $C_2^D(S)$.

S2: Connect each pair of PIs u in $C_1^D(S)$ and v in $C_2^D(S)$ such that $t(u) - t(v) = 1$ and $l(u) = l(v)$, and feed a new primary input w into them, where $l(u) = l(v)$ means that u and v are identical in S. □

For example, a DTEM $C^D(S_K)$ of S_K (Figure 2) is constructed as Figure 4 according to the above definition. Note that, after performing S2 of Definition 1, the value of 1 is added to all the label value of $C_2^D(S_K)$ in Figure 4. Also note that although two copies of CLB 1 in $t_{min}+1$ (also in $t_{min}+2$) can be merged into one CLB, $C^D(S_K)$ is expressed as Figure 4 to differentiate $C_1^D(S_K)$ and $C_2^D(S_K)$ from each other. If one wants to test the slow-to-rise fault on line l in S_K, test generation for one of the corresponding stuck-at 0 fault is performed on $C^D(S_K)$ under the constrained value of 0 that must be satisfied during test generation. In this way, transition tests for an acyclic sequential circuit can be generated by using a DTEM.

In [9], an acyclic sequential circuit is assumed to be obtained as a kernel circuit of a given circuit by using enhanced scan technique. Thereby, two consecutive vectors V_1 and V_2 to be applied to PPIs at the times corresponding to $t_{min}+1$ and $t_{min}+2$ in Figure 4 can be stored in ESFFs. Here, suppose a given circuit is designed by using standard scan technique. In this case, V_1 and V_2 for PPIs cannot be stored in SFFs but only V_1 can be stored. Consequently, V_2 must be justified by using some technique. In the next section, we discuss this problem.

3. Proposed Method

In this section, we discuss a new test generation model for broadside transition testing of partial scan circuits, and present a test generation method using the new model.

3.1 Broadside Test Generation Model

As pointed out in Section 2.2, vectors for PPIs in a frame, where

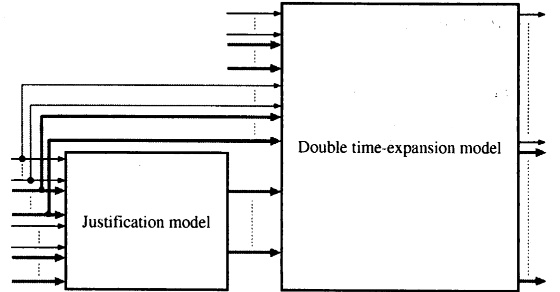

Figure 5: Overview of a broadside test generation model

a stuck-at fault exists, of a DTEM, must be justified by using some technique. Note that this frame is called a *test frame*. In order to achieve this requirement, we propose a *broadside test generation model*. The overview of a broadside test generation model is shown in Figure 5. A broadside test generation model is composed of a DTEM and a *justification model* which is used for the above requirement. The justification model and the broadside test generation model are defined as follows.

[Definition 2] Let S and S_K be a partial scan circuit and its kernel circuit, respectively. Let $C^T(S_K)$ and $C^D(S_K)$ be a TEM of S_K and a DTEM of S_K, respectively. Let t be the label value of a test frame in $C^D(S_K)$. Then, a combinational circuit obtained by performing the following procedure is said to be the justification model (JM) $C_t^J(S_K)$ with respect to t.

S1: For each PPI which belongs to only $C_2^D(S_K)$ in t, extract the logic cone of the corresponding PPO in $C^T(S_K)$. Also, for each PPI shared by $C_1^D(S_K)$ and $C_2^D(S_K)$ in t, extract the logic cone of the corresponding PPO in $C^T(S_K)$.

S2: For each pair of the logic cones, connect each pair of PIs (resp. PPIs) u in one cone and v in the other cone such that $t(u) = t(v)$ and $l(u) = l(v)$, and feed a new PI (resp. PPI) w into them. □

[Definition 3] Let S and S_K be a partial scan circuit and its kernel circuit, respectively. Let $C^D(S_K)$ and $C_t^J(S_K)$ be a DTEM of S_K and the JM with respect to the label value t of a test frame in $C^D(S_K)$.

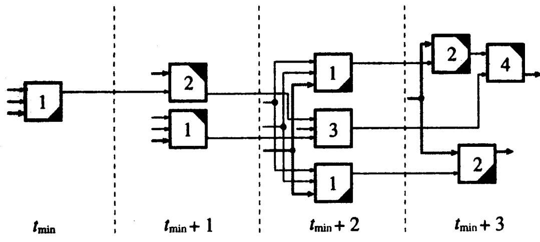

Figure 6: Justification model of $C^D(S_K)$: $C^J_{t_{min}+2}(S_K)$

Then, a combinational circuit obtained by performing the following procedure is said to be the broadside test generation model (BTGM) $C^B_t(S_K)$ with respect to t.

S1: For each PPI which belongs to only $C^D_2(S_K)$ in t, connect the corresponding PPO of $C^J_t(S_K)$ to the PPI. Also, for each PPI shared by $C^D_1(S_K)$ and $C^D_2(S_K)$ in t, connect the corresponding PPO of $C^J_t(S_K)$ to the PPI.

S2: Connect each pair of PIs (resp. PPIs) u in $C^J_t(S_K)$ and v in $C^D(S_K)$ that $t(u) = t(v)$ and $l(u) = l(v)$, and feed a new PI (resp. PPI) w into them. □

Notice that, for a given circuit, $d+1$ JMs are created, where d denotes the sequential depth of its kernel circuit. Hence, $d+1$ BTGMs are also created.

Figure 6 shows the JM $C^J_{t_{min}+2}(S_K)$ of Figure 4. This JM is composed of the logic cone of the PPO of CLB 4 in $t_{min}+3$ (Figure 3) and that of the PPO of CLB 2 in $t_{min}+3$. Note that although those two logic cones can share CLBs 1 and 2, we explicitely express the two logic cones for simplicity. Figure 7 shows the BTGM $C^B_4(S_K)$ of Figure 4. In creating this BTGM, the value of 2 is assigned to t_{min} of Figure 4 and the value of 0 is also assigned to t_{min} of Figure 6. As shown in Figure 7, CLBs in a frame are not shared to differentiate the DTEM and the JM. Patterns that are needed to activate stuck-at faults in a test frame and propagate those effects to a PO or a PPO can be justified by using its JM.

3.2 Test Generation Flow

Given a partial scan circuit S whose kernel circuit S_K is acyclic, broadside transition tests for S are generated as follows:

S1: Create a transition fault list F^T of S.

S2: Construct $d+1$ BTGMs $C^B_{t_1}(S_K), \ldots, C^B_{t_{d+1}}(S_K)$ of S_K, where d is the sequential depth of S_K.

S3: Create stuck-at fault lists F^S_1 for $C^B_{t_1}(S_K)$,..., F^S_{d+1} for $C^B_{t_{d+1}}(S_K)$ corresponding to F^T, and constrained value lists C_1 for F^S_1 ,..., C_{d+1} for F^S_{d+1}.

S4: For each stuck-at fault $f^S \in F^S_i$ $(i = 1, \ldots, d+1)$,

(a): generate a test pattern t^S under the corresponding constraint $c \in C_i$, and

(b): transform t^S into a broadside test t^T for the corresponding transition fault $f^T \in F^T$ according to the label information of $C^B_{t_i}(S_K)$.

Note that, in S3, even if a transition fault in a given circuit corresponds to some stuck-at faults in its BTGMs, we can handle the respective stuck-at faults one by one because generated broadside transition tests are applied in the slow-fast-slow testing manner. In S4, if all the stuck-at faults corresponding to a transition fault are identified as untestable, the transition fault is also untestable. Moreover, it is sufficient to generate a test pattern for one of the stuck-at faults corresponding to a transition fault. In S4 (b), t^S is transformed into t^T as follows. For example, in Figure 7, a pattern for each of the PIs and the PPI of CLB 1 in frame 0 is transformed into a pattern for each of the PIs of CLB 1 and the corresponding SFF at time 0 in Figure 2. Notice that, the pattern for the SFF is set by scan-in operation before time 0. Other patterns in frames from 1 to 6 are transformed in the same way.

The following theorem shows the correctness of our test generation method.

[Theorem 1] Let S and S_K be a partial scan circuit and its kernel circuit, respectively. Let $f^T_\uparrow$ (resp. $f^T_\downarrow$) be a slow-to-rise (resp. slow-to-fall) transition fault in S. Let $F^S_{\text{s-a-0}}$ (resp. $F^S_{\text{s-a-1}}$) be the set of stuck-at 0 (resp. 1) faults corresponding to $f^T_\uparrow$ (resp. $f^T_\downarrow$). Then, $f^T_\uparrow$ (resp. $f^T_\downarrow$) is testable under the broadside testing manner if and only if at least one $f^S_{\text{s-a-0}} \in F^S_{\text{s-a-0}}$ (resp. $f^S_{\text{s-a-1}} \in F^S_{\text{s-a-1}}$) in the corresponding BTGM $C^B_t(S_K)$ is testable under the constrained value of 0 (resp. 1).

[Proof] Broadside transition test generation for $f^T_\uparrow$ (resp. $f^T_\downarrow$) in S can be viewed as test generation for the stuck-at 0 (resp. 1) fault in S corresponding to $f^T_\uparrow$ (resp. $f^T_\downarrow$) in a situation where (a) the constrained value of 0 (resp. 1) must be set to the faulty site at time t_{1st}, and (b) no scan operation must be performed between t_{1st} and t_{2nd}. Here, t_{2nd} denotes a time at which the stuck-at 0 (resp. 1) fault in S is activated, and $t_{1st} = t_{2nd} - 1$. In [17], it has been shown that the stuck-at test generation problem for an acyclic sequential circuit can be reduced to that for its TEM. The properties of a TEM still hold in a BTGM because the BTGM is constructed by using the TEM. Hence, we can demonstrate this theorem by showing that (a) and (b) are satisfied in test generation for the BTGM. Since, in $C^B_t(S_K)$, stuck-at test generation for $f^S_{\text{s-a-0}}$ (resp. $f^S_{\text{s-a-1}}$) is performed under the constrained value of 0 (resp. 1), (a) is satisfied. Furthermore, since patterns for $f^S_{\text{s-a-0}}$ (resp. $f^S_{\text{s-a-1}}$) in the test frame of $C^B_t(S_K)$ are justified by its JM, (b) is also satisfied. Thus, the theorem is proved. □

3.3 Test Application

In this subsection, we describe how to apply broadside transition tests to a partial scan circuit.

Broadside transition tests generated by the method of Section 3.2 are applied to a partial scan circuit S whose kernel circuit S_K is acyclic as follows. Let $C^D(S_K)$ be a DTEM of S_K, and t be the label value of a test frame. In test application, the circuit is operated at a slow clock speed except when its rated clock is applied at the

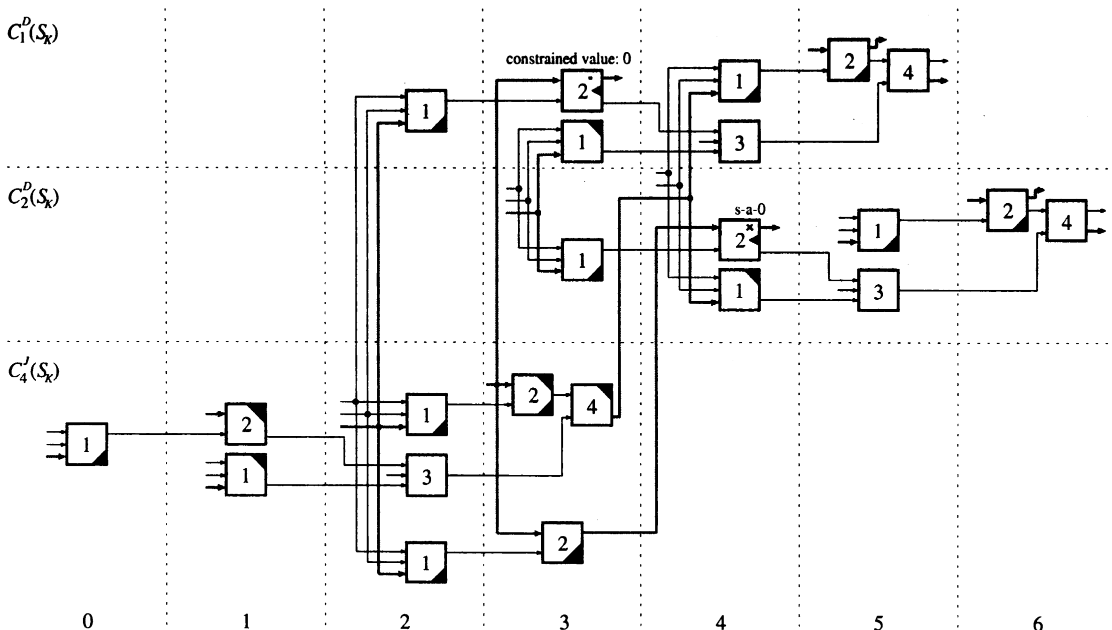

Figure 7: Broadside test generation model of $C^D(S_K)$: $C_4^B(S_K)$

time corresponding to t. If there exists a PPI in a frame before the test frame, scan-in operation is performed before the corresponding time. Also, if there exists a PPI which belongs to only $C_2^D(S_K)$ in a frame after the test frame t, scan-in operation is performed before the corresponding time. Scan-out operation is performed after the corresponding time if there exists a PPO which belongs to only $C_2^D(S_K)$ in a frame between the test frame t and the last frame. Note that, in order to keep the values of normal FFs during scan operation, the system clock must be separated from the scan clock or all the normal FFs have to be redesigned such that the values can be held during scan operation. For example, a broadside transition test generated by performing test generation on the BTGM $C_4^B(S_K)$ shown in Figure 7 is applied to the partial scan circuit shown in Figure 1 as follows. Scan-in operation is performed before each time from 0 to 3, then the circuit is operated at a slow clock speed. The transition to activate transition faults is created between times 3 and 4, then between times 4 and 5, its fault effect is captured at the rated clock speed. Before each time of 5 and 6, scan-in and scan-out operations are performed simultaneously, then the circuit is operated at the slow clock speed. After time 6, scan-out operation is performed. Let d be the sequential depth of S_K. The length of a broadside transition test can range from $d+2$ to $2d+2$. In the case of Figure 2, it ranges from 5 to 8.

4. Experimental Results

In this section, we evaluate the proposed method in terms of area overhead, over-testing and test generation time.

The following experiment was performed on a PRIMEPOWER 650 workstation (Fujitsu, CPU: SPARC64 V 1.35GHz × 4, Memory: 16GB). TetraMAX ATPG (Synopsys) was used as a test generation tool with a backtrack limit of 100. We applied our method to a sample circuit that is composed of several ISCAS '85 benchmark circuits. This circuit is constructed as Figure 1, and CLBs 1, 2, 3 and 4 correspond to c5315, c7552, c3540 and c6288 of the ISCAS '85 benchmark circuits, respectively. The characteristic of this circuit are shown in Table 1. In Table 1, columns "#PIs," "#POs" and "#FFs" denote the number of PIs, POs and FFs, respectively. Column "Area" denotes the area of the circuit estimated by Design Compiler (Synopsys), where the area of a 2-input NAND gate is considered to be 2. We compared the proposed method to a fully enhanced scan method and a full scan method in this experiment.

Table 1: Circuit characteristic of a sample circuit

#PIs	#POs	#FFs	Area
198	16	257	20,359

First, we show area overheads needed for the three methods considered. In the fully enhanced method and full scan one, their area overheads were +21.5% and +8.8%, respectively. Our method only required an area overhead of +3.4% to make the kernel circuit acyclic. Since the proposed method is based on partial scan design, we can achieve low area overhead compared with the other methods.

Next, we show test generation results. In this experiment, we compared the test generation time and the number of untestable faults in our method with those in the other two methods when every method reached 100% fault efficiency for targeted transition

Table 2: Test generation results for a sample circuit

Method	#faults	#det	#unt	TGT [s]
Enhanced scan		37,237	61	194.21
Full scan	37,298	37,210	88	285.97
Our method		37,178	120	883.09

faults. Table 2 lists the test generation results obtained by the fully enhanced scan method, full scan one and proposed one, which are denoted by "Enhanced scan," "Full scan" and "Our method" respectively. Columns "#faults," "#det" and "#unt" give the number of targeted transition faults, detected faults, identified untestable faults, respectively. Column "TGT [s]" denotes test generation time. In Table 2, "#unt" of "Enhanced scan" represents the number of combinationally untestable faults. In "Enhanced scan," the test generation time was the shortest because the test generation did not identify sequentially untestable faults. This may cause over-testing. In "Full scan," some sequentially untestable faults were identified although the test generation time increased. Since our method paid attention to more sequentially untestable faults by using BTGMs, the test generation time increased further. However, the number of identified sequentially untestable faults was the largest, and therefore this method can contribute to reducing yield loss caused by over-testing. Here, we evaluate the propose method further. As shown in [4], in broadside testing for a full scan circuit, the number of sequentially untestable faults identified during test generation increases as the number of time frames used by the test generation increases. This means that, in terms of over-testing, it is important to consider the behavior of a given circuit within a long time span during test generation. In our method, a time span from $d+2$ to $2d+2$ is considered during test generation, where d is the sequential depth of a kernel circuit. Therefore, compared with the conventional methods, it is conceivable that we can identify many sequentially untestable faults for more complex circuits as well as a simple circuit used in this experiment.

5. Conclusions and Future Work

In this paper, we proposed a method of broadside test generation for transition faults in partial scan circuits. To generate broadside transition tests for a partial scan circuit whose kernel circuit is acyclic, we transform the kernel circuit into some combinational circuits called broadside test generation models. Then, all the broadside transition tests are generated by performing constrained stuck-at test generation on the broadside test generation models. Through experiments, we showed that out method can reduce over-testing in reasonable test generation time compared with the previous methods.

Our future work is to handle a more general delay fault model, i.e., the path delay fault model, in this frame work.

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