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# LSIブロックのための柔軟な電力遅延マクロモデルの提案

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**あらまし** ポータブル機器の急速な普及に伴い，電池のサイズを増大させることなく電池寿命を長くすることは非常に重要な課題となっている．特に，ユビキタス・コンピューティング時代においては，厳しいサイズ制約における電池の長寿命化が強く求められる．本稿では，電池の消耗・回復と出力電圧の経時降下を表現する高精度なモデル化手法について提案する．性能の異なる電池に対する設計最適化方法に関して計算機実験による評価結果について議論する．

**キーワード** 電池駆動システム，低電力，電源最適化，電池モデル

# A Flexible Power and Task Modeling for LSI Blocks

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**Abstract** Due to the rapid popularization of portable equipments, it becomes very important to make the battery lifetime longer without increasing the total system size. Especially toward the ubiquitous computing age, long battery lifetime in a tight size limitation will be highly required. This paper proposes a new flexible power and task models of the LSI. Practical battery model which represents output voltage decline as well as recovery of charge by the length of rest time is also proposed. These models help effective design explorations of small size systems.

**Keyword** system operated by batteries, low power, power dissipation model, battery model

## 1. Introduction

To the advent of ubiquitous computing era, much smaller size and systems operated by battery will take a large space in the major electric market. It will be an important new objective to maximize the battery lifetime in a tight size restriction for those systems, and is not equal to the conventional goal which minimize the power consumption only.

In conventional design flow of systems operated by battery, the battery selection and the power converter design are located in late phases of the flow. This sometimes leads to serious violations of lifetime/weight specifications, and imposes redesign. [2,5]

The figure 1 depicts the typical structure of the power supply systems, which consists of the LSI circuit, the battery cell, and the buck converter. The $V_{dd}$ and $I_{dd}$ are the supply voltage and current of the LSI. The $V_{in}$ and $I_{in}$ are discharged voltage and current from the battery.

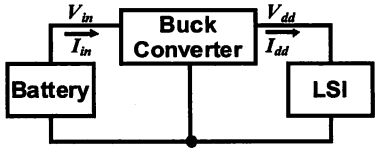


Fig. 1. Circuits structure of battery-powered digital systems

Main components of the system are the battery, the converter with external devices (an inductor

and a capacitor), and the LSI. The total size to mount all of these components is fixed, and there are very complicated trade-off relationships between them. For example, the size of external devices of the converter is reduced if the switching frequency of the converter were increased. Then, the battery size is increased, and the battery capacitance and the lifetime may be increased. At the same time, the power consumption of the converter is increased and that may cause the reduction of the battery lifetime.

There is another example, that the power consumption of the LSI may be reduced by decreasing the power supply voltage. However, at the same time, the battery lifetime can be increased if adequate recovery time is given to the battery by increasing the length of the rest time. It is because the length of the active time can be reduced by speeding up the LSI operation by increasing the power supply voltage.

To solve the complicated trade-off optimization problem, the authors have developed a spontaneous optimization scheme of the battery, the converter, and the LSI, and it has been shown that the design point of battery lifetime maximization is not always equal to that of LSI power minimization [1]. However, the design models introduced in the prior work were not very accurate enough to practical designs.

This paper focuses on the design modeling issues, and proposes a new flexible power, delay, and task models of RTL blocks of LSI in this system. It also proposes a new practical model of battery which represents output voltage decline as well as recovery of charge by the length of rest time. We have newly defined the task model that is required for the system behavior. The optimization objective is formulated to maximize the battery life time by exploring the design space of the $V_t$, $V_{dd}$, MTCMOS option, clock frequency, active/standby ratio, etc., in the restriction of the predefined tasks. These accurate models enable reliable optimization.

## 2. Design Platform for Small Size Systems Operated by Battery

For ultra low power applications, it is effective that the LSI has active and standby mode. For example of medical micro capsular robots, the LSI executes communications with the host computer, image code compressions, and image captures in active mode. In such applications, the usual workload, e.g. number of pictures taken in a constant time, is predefined. We define those work loads as tasks.

As known, the power consumption of digital circuits are represented by the following formula.

$$P = \sum \left( \alpha \cdot f \cdot C \cdot V_{dd}^{\ 2} + I_{sc} \cdot V_{dd} + I_{leak} \cdot V_{dd} \right) \quad \cdots\cdots (1)$$

The first term is the dynamic power consumption, α is the switching probability. The second term is the short circuit power consumption when the gate does the switching momentarily at the time of turn on PMOS and NMOS. It can be ignored in well tuned designs since repeaters are adequately inserted in such designs. The third term is the leak power. It consumes 30% or more of the LSI in recent years. The leak current, and the delay time between gate to gate are formulated by the formula (2), and (3), respectively.

$$I_{leak} = I_0 \cdot \exp\left( \frac{-q \cdot V_t}{n \cdot k \cdot T} \right) \quad \cdots\cdots (2)$$

$$T_{Delay} = K \cdot \frac{V_{dd}}{(V_{dd} - V_t)} \quad \cdots\cdots (3)$$

### *A) Operation Mode of the LSI*

The figure 2 depicts the electric current consumption model of the LSI of active or standby mode. High supply voltage $V_{dd}$ makes the execution time shorter but it increases dynamic power consumption. It increases the $I_{dd\_act}$ increased and decreases the active time ratio $D_i$. The situations are opposite in case of low supply voltage.

Low threshold voltage $V_t$ makes the execution time shorter but it increases standby power consumption. It increases the $I_{dd\_standby}$ and decreases the active time ratio $D_i$. The situations are opposite in case of high threshold voltage.

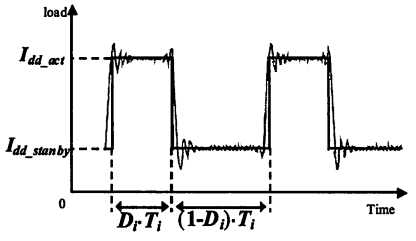


Fig. 2. Current model of the LSI

This system assumes that the power consumption and the processing speed of the each block can be controlled by changing the values of $V_{dd}$ and $V_t$ independently. It assumes that some blocks have option to be designed with the circuit architecture of VTCMOS[9,12] or MTCMOS[11]. The $V_t$ can be changed dynamically by using the VTCMOS. On the other hand, he power consumption of the block can be completely stopped at standby mode by using the MTCMOS.

### *B) Task Model of the LSI*

Several tasks are executed. The concept of the task is similar to the process in the Electric System Language, e.g. in System C. The task model is

newly introduced to define the work loads of system. In a case of medical diagnosis systems, taking a picture or transmitting a status data corresponds to those tasks. The optimization objective is to maximize the battery life time in the situation of the predefined tasks.

Each task is defined by the number of clocks to execute, critical path delay for clock synchronization, and ***P***, ***D***, ***SC*** values of each block which is calculated by behavior analysis of signals. The ***P*** is the probability that the value of the pin equal to "1". The ***D*** is the mean value of number of logic value changes. The ***SC*** represents temporal and geometrical distribution.

The macro model of the each block of LSI consists of critical path delay, dynamic and static power consumption model which are parameterized by power supply voltage and transistor threshold voltage. This power consumption is calculated by considering the switching activity defined by the tasks

### *C) Design Optimization Scheme*

The design platform is organized by battery, converter, and LSI models, and combinatorial optimizer. Each model is calculated by the mathematical formula or look-up-table.

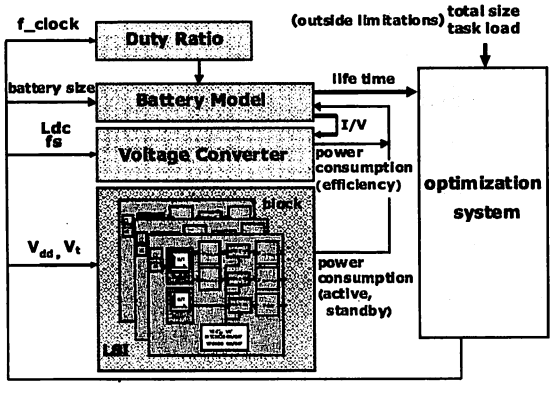


Fig.3. Design optimization scheme

Figure 3 depicts the system organization of the design platform. The battery model is characterized by some parameters which specify the total capacity, recovery capability, and voltage decline caused by electric current. The duty ratio, i.e. active/standby ratio, influences to the battery recovery characteristic, too. The duty ratio, i.e. active/standby ratio, influences to the battery recovery characteristic, too. The output of the battery model is lifetime length and the output voltage decline characteristics.

The inputs of the converter are the switching frequency, the external device sizes, and input voltage. The output of the converter is the power consumption.

The inputs of the LSI are $V_{dd}$, $V_t$, MTCMOS and VTCMOS options. The values ***P***, ***D***, ***SC*** are given to each RTL blocks to calculate the active power consumption.

The optimization algorithm is formulated by the evolutionary algorithm since it is considered suitable for multi-objective optimization. The evolutionary algorithm has ***n*** states. The each state corresponds to a combination of the values of all design parameters. Small modification to a parameter selected randomly is applied to make new ***n*** states. In the ***2 * n*** states, old ***n*** states plus new ***n*** states, the algorithm select ***n*** states that gives larger battery lifetime [1].

## 1. 3. Macro Model for LSI Blocks

### *A) Power Consumption Model for Variable $V_{dd}$ and $V_t$*

From the formulas (1,2), if the dynamic power $P_{dynamic}$ and leak power $P_{leak}$ were calculated for a power supply voltage $V_{dd}$ and a transistor threshold voltage $V_t$, then the dynamic and leak power of different power supply voltage $V_{dd}'$ and threshold voltage $V_t'$ are calculated by the following formulas.

$$P_{dynamic}(V_{dd}') = P_{dynamic} \times \frac{(V_{dd}')^2}{(V_{dd})^2} \quad \cdots\cdots\cdots (3)$$

$$P_{leak}(V_{dd}', V_t') = P_{leak} \times \frac{e^{-\Delta V_t'}}{e^{-\Delta V_t}} \times \frac{(V_{dd}')^2}{(V_{dd})^2} \quad \cdots\cdots (4)$$

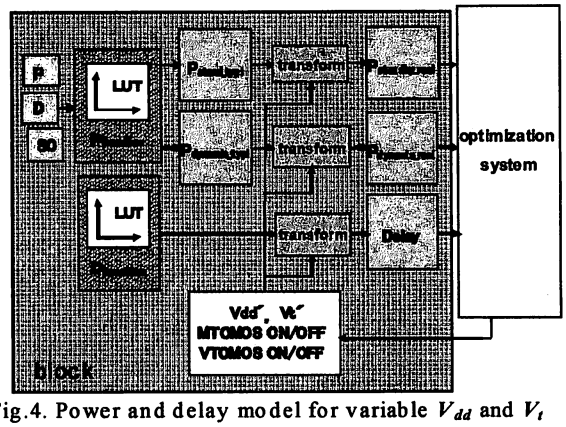


Fig.4. Power and delay model for variable $V_{dd}$ and $V_t$

The power and delay model of a resister transfer level, RTL in short, block is illustrated in the figure

4. This model provides a mechanism to estimate the dynamic power of the block, which seeks the active power consumption by table-look-up manner. The parameters of the table are ***P***, ***D***, ***SC***, i.e. switching activities. The active power estimation algorithm is similar to a conventional approach. It constructs the look-up-table parameterized by ***P***, ***D***, ***SC***, by iterating a switch level simulator many times. The leak power estimator estimates the number of transistors by Lents law, and calculates the $\Sigma I_0$ of the formula (2).Each block is linked to the optimization system, same as that in the figure 2, the optimizer observes the active and leak power. Sets of {***P***, ***D***, ***SC*** } which corresponds to the usual tasks is given to the block. The optimizer modify the values of $V_{dd}$ and $V_t$ to explore the design space.

### *B) Power Consumption Model for MTCMOS*

The power consumption model with or without the MTCOS is shown below. In the MTCMOS circuit, inner low threshold voltage transistors are sandwiched by high threshold voltage transistors at their top and bottom. The $V_{dd\_eff}$ is the effective power supply voltage for inner low threshold voltage transistors.

**(i) With MTCMOS**

$$P_{0A} = fV_{dd-eff}{}^2 \Sigma\alpha \cdot C + V_{dd-eff} \cdot \Sigma I_o \exp\left(\frac{-q(V_{gs}-V_{tL})}{n \cdot k \cdot T}\right) \quad (5)$$

$$D_{0A} = \frac{C \cdot V_{dd-eff}}{k_2 (V_{dd-eff} - V_{tL})} \quad (6)$$

$$P_{0S} = V_{dd-eff} \cdot \Sigma I_o \exp\left(\frac{-q(V_{gs}-V_{tH})}{n \cdot k \cdot T}\right) \quad (7)$$

$$V_{dd-eff} = V_{dd} - V_{tHp} - V_{tHn} \quad (8)$$

**(ii) Without MTCMOS**

$$P_{1A} = fV_{dd}{}^2 \sum \alpha c + V_{dd} \cdot \Sigma I_o \cdot \exp\left(\frac{-q(V_{gs}-V_{tL})}{n \cdot k \cdot T}\right) \quad (9)$$

$$D_{1A} = \frac{C \cdot V_{dd}}{k_2 (V_{dd} - V_{tL})} \quad (10)$$

$$P_{1S} = V_{dd} \cdot \Sigma I_o \cdot \exp\left(\frac{-q(V_{gs}-V_{tL})}{n \cdot k \cdot T}\right) \quad (11)$$

### *C) Delay Model*

A simple delay model has been used in conventional approaches as shown in (12).

$$T_{Delay} = K \cdot \frac{V_{dd}}{(V_{dd} - V_t)} \quad (12)$$

This paper newly propose a more accurate delay model. Firstly, a comparison of the delay calculated with the previous model of Eqn. (12) and measured with HSPICE is shown in Figure 5. A series of 10 inverters was used for measurement to represent a critical path of a logic design. It is obvious that previous model fails to reproduce a characteristic of delay as a function of $V_{dd}$.

We will now derive a more accurate delay model. The delay equation follows from the current equation:

$$i = C \cdot \frac{dV}{dt}$$

$$\Delta t = C \cdot \frac{dV}{I_{ds}} = C \cdot \frac{V_{dd}/2}{K \cdot (V_{dd} - V_t)^{\alpha}}$$

$$I = K \cdot (V_{dd} - V_t)^{\alpha} \quad (13)$$

$$K = \mu \cdot C_{ox} \cdot \frac{W}{L} \quad (14)$$

$$\tau = \sum_{i=1}^{n} \Delta t_i \quad (15)$$

where $\mu$ is effective mobility, $C_{ox}$ is oxide capacitance, $W$ and $L$ are channel width and length. Eqn. (13) is obtained from [16]. Here, $\tau$ is total delay in critical path of LSI which is composed of the sum of the delay of each gate. $\alpha$ is closely related with the velocity saturation of carriers, $\alpha$ can be called a velocity saturation index. The delay can be predicted by changing the $\alpha$ to an appropriate value to fit experimental results.

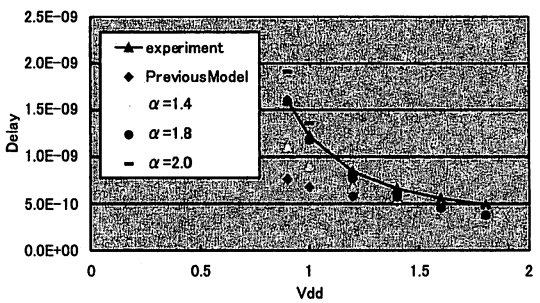


Figure 5 Delay vs. Vdd

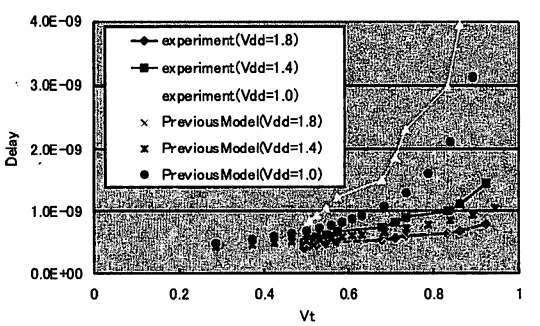


Figure 6 Comparison of delay of experiment and calculated with the previous model.

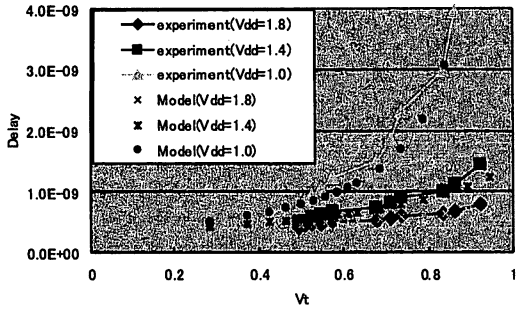


Figure 7 Comparison of delay of experiment and calculated with the modified model with $\alpha$=1.2.

The delay must be modeled accurately, not only when ***Vdd*** changes, but also when ***Vt*** changes. Figure 6 shows this effect where an exponential relationship exists between the delay and the threshold voltage. According to Figures 5 and 7, a suitable value for $\alpha$ is the range of 1.0 – 1.3. In this experiment on 0.18um, Figure 7 shows the suitable value for $\alpha$ is around 1.2. The appropriate value should be obtained using HSPICE on the target technology using a chain of inverters.

## 4. Macro Model for Batteries

### *A. Battery Model* [5-8]

Important characteristics of a battery is that some amount of energy will be wasted when the battery delivers the energy required for the circuit. The efficiency of the battery $\eta_{bat}$ is given by a function of discharged current $I_{in}$. [2]

$$\eta_{bat} = 1 - h \cdot I_{in} \quad \text{.....(16)}$$

In this formula, $h$ is a constant value given for each battery. Rakhmatov define the total capacitance consumption of a battery of time $t$ by $\sigma(t)$. [5]

$$\sigma = \int_0^t i(\tau)d\tau + \int_0^t i(\tau)\left(2\sum_{m=1}^{\infty} e^{-\beta^2 m^2 (t-\tau)}\right)d\tau \quad \text{.....(17)}$$

Note that the first term is efficiently used for output load, but the second term can not be pull out of the battery. By using (16) and (17),

$$\sigma = \left\{\int_0^t \frac{i(\tau)}{1-h\cdot i(\tau)}d\tau + \int_0^t \frac{i(\tau)}{1-h\cdot i(\tau)}\left(2\sum_{m=1}^{\infty} e^{-\beta^2 m^2 (t-\tau)}\right)d\tau\right\} \quad \text{.....(18)}$$

Once the battery capacitance ***CAP*** is defined, the battery lifetime ***Tlife*** is caluculated by the formula (19). In this formula, $\beta$, $h$ are important parameters to characterize a battery.

$$CAP = \left\{\int_0^{Tlife} \frac{i(\tau)}{1-h\cdot i(\tau)}d\tau + \int_0^{Tlife} \frac{i(\tau)}{1-h\cdot i(\tau)}\left(2\sum_{m=1}^{\infty} e^{-\beta^2 m^2 (Tlife-\tau)}\right)d\tau\right\} \quad (19)$$

The ***CAP*** is proportional to the battery size ***Size_bat***, and given by,

$$CAP = a\cdot(Size\_bat - b) \quad \text{.....(20)}$$

$a$, $b$ are constant values.

In the figure 8 and 9, the top picture shows electric current consumption, and the bottom picture shows the charge remained in the battery. The figure 8 is the case when the battry recovery time is sufficient, and the battery is effectively used. The figure 9 is the case when the battry recovery time is not sufficient, and the battery is quickly wasted.

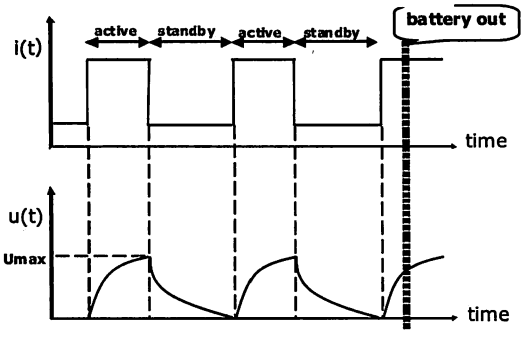


Fig. 8 The battery model (1)

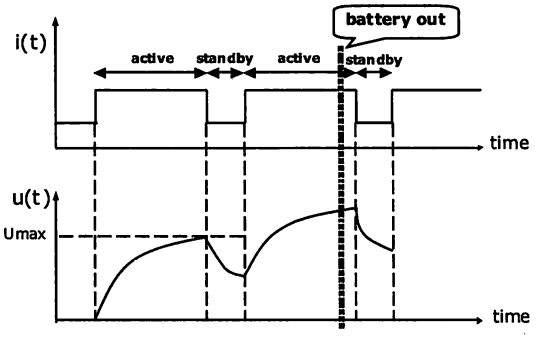


Fig. 9 The battery model (2)

Additionally, we have introduced internal resistance model which represents voltage decline curve. The model is implemented by adding a inner resistance.

## 5. Experimental Results

To evaluate the effect of this proposal technique, we optimized operation parameters of battery, converter and LSI by the evolutionary algorithm. It maximize the battery lifetime in the restriction of total size, by simultaneous consideration of operation condition of battery, buck converter, and LSI, selection of MTCMOS, VTCMOS. The results are compared with manual optimization, shown in the tables 1 and 2.

The results show our approach finds better solution in terms of battery life time, etc. We have found that VTCOS and MTCMOS options are adequately selected. Also optimum value of duty is selected by optimum frequency of LSI that is calculated by more accurate delay model that we proposed in the section3.

Table 1. The resolution of optimization

| | Power consumption | Duty ratio | Delay | Battery lifetime |
|---|---|---|---|---|
| Auto | 9.96E-05 | 0.69 | 1.20E-05 | 2.59E+06 |
| Manual | 1.10E-04 | 0.69 | 1.20E-05 | 2.51E+06 |

Table 2. Experimental result

| | | Vt | Power consumption | Duty ratio | Delay | Battery lifetime |
|---|---|---|---|---|---|---|
| Manual | | 0.6 | 1.73E-04 | 0.69 | 1.20E-05 | 1.46E+06 |
| VIDEO, SENSOR | (Auto) | 0.65 | 1.74E-04 | 0.70 | 1.15E-05 | 3.23E+06 |
| DRIVE,I/O, MPU | | 0.6 | | | | |

## 6. Conclusion

We have proposed a new flexible power and task models of the LSI. Practical battery model which represents output voltage decline as well as recovery of charge by the length of rest time is also proposed. We have proposed the accurate delay and power model of RTL blocks which is applicable to flexible power supply voltage and transistor threshold voltage.

Unfortunately, the results of the delay model show we have not derived appropriate common value $\alpha$ and $\beta$ yet. However, we intend to propose the concept of the model for , the platform in this paper. We are prepared to do more experiments and find more accurate parameter fitting methodology until the final paper. These models help effective design explorations of s mall size systems.

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