計算機アーキテクチャ　98－18
設　計　自　動　化　65－18
（1993. 1. 22）

超高性能PA-RISCプロセッサチップのアーキテクチャ

PA7100-最適化RISC 設計

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あらまし

PA-RISCプロセッサチップは世界で最も高速のシングルチッププロセッサに属する。

本セッションでは、このPA-RISCプロセッサについて、まず簡潔に設計におけるトレードオフを数例紹介し、それから命令セットの最適化、パイプラインデザイン、そして大容量かつ高速の外部キャッシュメモリの設計について討議を進める。

また、テクノロジーのトレンドが、この先１０年の間に、PA-RISCプロセッサのデザインやパフォーマンスにどのような影響を与えるのか、考察する。

和文キーワード

The Architectuer of PA-RISC Processor Chip

PA7100-An Optimized RISC Design

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Abstract

This talk, on *The Architecture of PA-RISC Processor Chips*, will briefly review some of the design tradeoffs which have made PA-RISC Processors among the fastest single-chip processors in the world. It will discuss optimization of the instruction set, the pipeline design, and designs for very fast, large external caches.

We will also examine how technology trends will affect RISC processor design and performance during the rest of these decade.

英文 key words

The Architecture of PA-RISC Processor Chips

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PA7100

AN OPTIMIZED RISC DESIGN

BASIC PERFORMANCE CRITERIA

$$MIPS = \frac{CLK}{CPI}$$ ➡ "TACHOMETER"

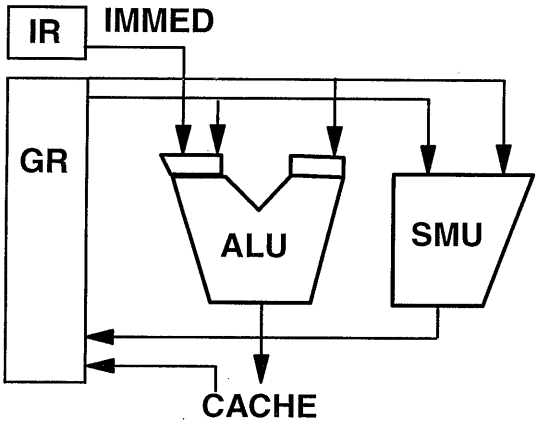
$$THROUGHPUT_a = \frac{CLK}{P_a \times CPI}$$ ➡ "SPEEDOMETER"

P = Path, # Of Instructions Executed
CPI = Average Machine Cycles/Instruction
CLK = Clock Speed (Megahertz)

PA-RISC METHODOLOGY

- **DATA-DRIVEN**
  Based on voluminous traces of many applications representing many computing environments:
  - Technical and Commercial
  - Single-user and Multi-user
  - Interactive, Batch, and Real-Time
- **ITERATIVE DESIGN**
  - Postulate architecture
  - Simulate functionality, compilers, hardware
  - Evaluate cost/performance
- **OPTIMIZE COST / PERFORMANCE**

SIMPLE DATAPATH



PA-RISC DIFFERENTIATORS

- HUGE GLOBAL VIRTUAL ADDRESS SPACE
- ROBUST PROTECTION MECHANISM FOR CODE AND DATA
- COMBINED-OPERATION INSTRUCTIONS
- EFFICIENT SUPPORT FOR ALL IMPORTANT DATA TYPES

PA-RISC COMBINED-OPERATION INSTRUCTIONS

- LOAD/STORE WITH BASE MODIFICATION
- COMPARE AND BRANCH, ADD AND BRANCH, MOVE AND BRANCH
- EXTRACT (SHIFT AND MASK), DEPOSIT (SHIFT AND MERGE)
- FLOATING MULTIPLY AND ADD, MULTIPLY AND SUBTRACT
- UNIT ADD, UNIT EXCLUSIVE-OR

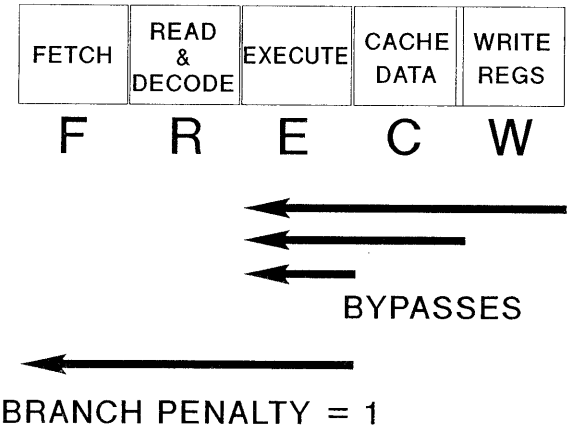
SPEC Instruction Count Ratios

(Normalized to PA-RISC = 1)

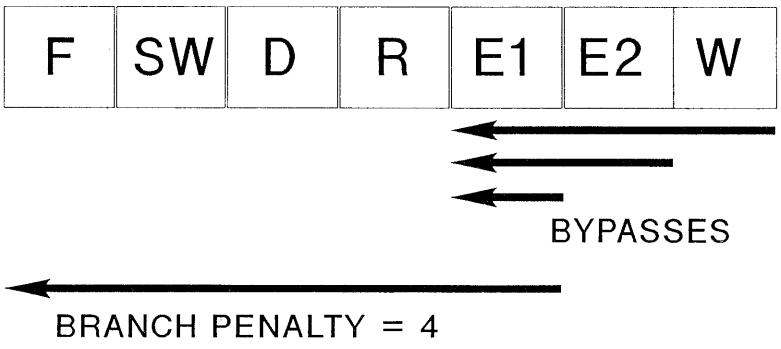
	SPARC/PA	MIPS/PA
Floating-Point	1.60	1.84
Integer	1.35	1.18
Total	1.50	1.54
Total (-matrix300)	1.37	1.36

(Smaller is Better)

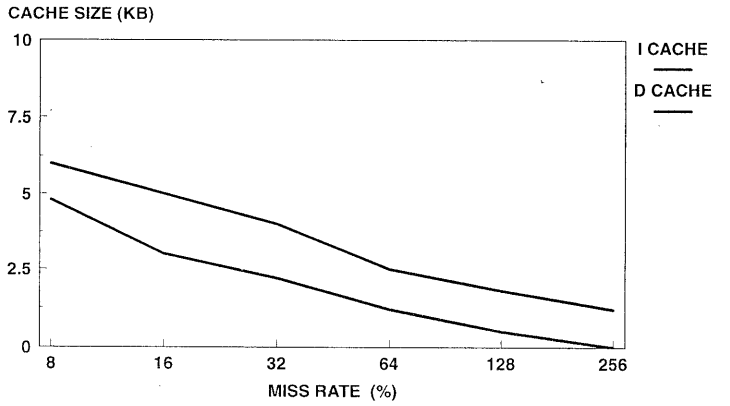
PA 7100 PIPELINE



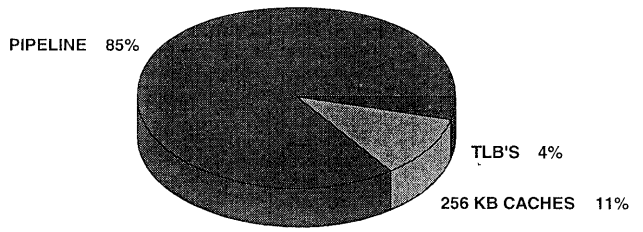
COMPLEX PIPELINE



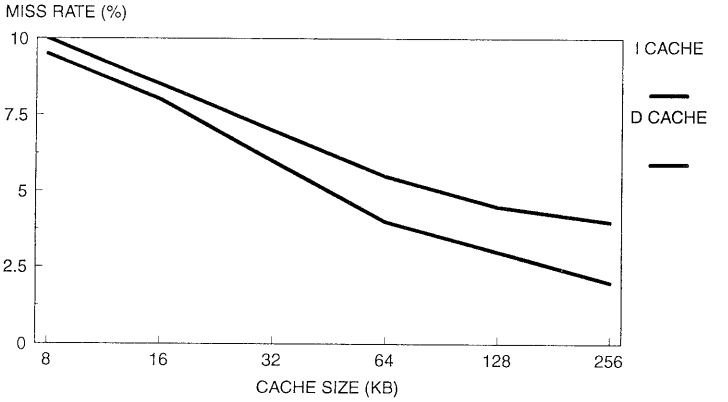
SPEC GCC



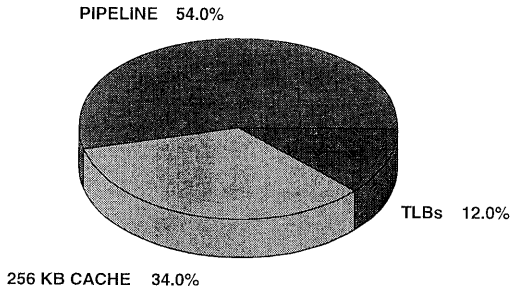
SPEC GCC CPI



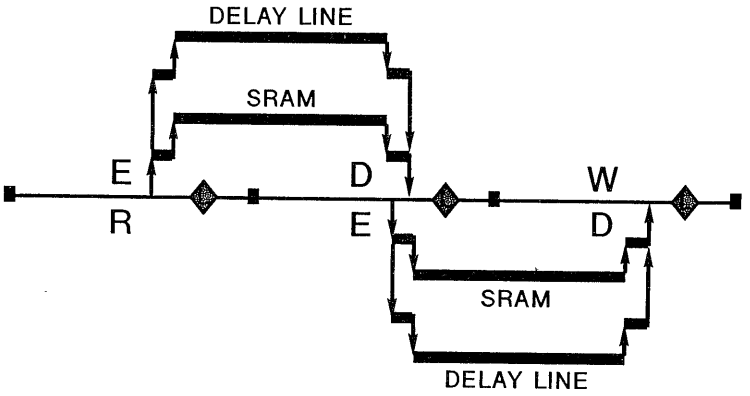
TRANSACTION PROCESSING



TRANSACTION PROCESSING CPI



AGGRESSIVE CACHE TIMING



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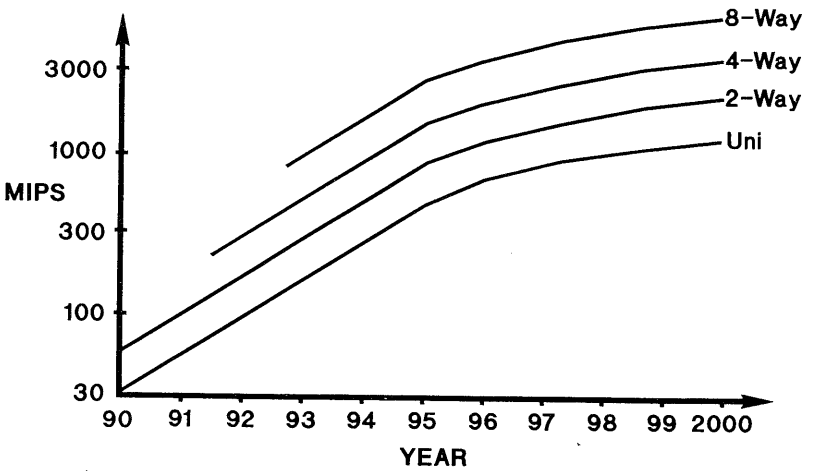
PROCESSOR PERFORMANCE GROWTH



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