RC Extraction-free Wiring Delay Analysis Focusing on Number of On-state Switches for Via-switch FPGA

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Abstract: Conventional SPICE-based timing analysis with RC extraction is time consuming for RC wiring delay analysis. This paper proposes a wiring delay model that is expressed as a function of the numbers of on-state switches and signal distance for via-switch FPGA, which makes RC extraction and SPICE simulation unnecessary. Experimental results show that the proposed modeling achieves only 1.74% error on average for single-fanout samples compared with SPICE simulation. As for two-fanout cases, the proposed modeling also attains 1.77% error on average.

Keywords: wiring delay model, interconnect delay analysis, via-switch FPGA

1. INTRODUCTION

Field-programmable gate array (FPGA) is superior to application-specific integrated circuit (ASIC) in terms of design effort and turn-around time. However, FPGA interconnect consists in memory elements, buffers and routing multiplexers, rather than a simple metal wire as in ASICs [1]. In recent FPGAs, Static Random Access Memory (SRAM) has been mainly used to store the select signals of multiplexers and the on/off state of the transmission gate [2]. Via-switch FPGA, a kind of RRAM-based FPGA, which uses via-switches to configure crossbar, is different from conventional SRAM FPGA in interconnect structure [3]. Signal routing is enabled by crossbars where each intersection of vertical and horizontal lines has a nonvolatile switch, and no multiplexer or transmission gates are used. Consequently, via-switch FPGA enables more complex wiring topologies than conventional FPGA while via-switch FPGA is based on an array-based regular structure. Therefore, the delay analysis for conventional FPGA is not applicable to via-switch FPGA.

Fig. 1 shows a wiring delay analysis flow that mainly consists of equivalent circuit construction with RC extraction and circuit analysis for delay computation. Wiring delay can be analyzed accurately by creating an equivalent RC circuit model corresponding to an actual wiring pattern and using a circuit simulator such as HSPICE. However, it takes a huge amount of time to analyze a large number of wiring patterns. Therefore, fast yet accurate delay analysis techniques are demanded.

Here, there are two approaches for fast wiring delay analysis. The first approach is to simplify the equivalent circuit for shorter simulation time. In [5], the authors simplified the equivalent circuit for via-switch FPGA within 1.8% average error such that programming lines are removed, off-state via-switches are replaced with capacitances, and finally a smaller circuit with fewer π structures is synthesized. Consequently, 52x and 49x speed-ups are achieved for single-fanout paths and multiple-fanout paths, respectively. The other approach is to adopt a sophisticated interconnect analysis methods for delay estimation, such as AWE and PRIMA [6, 7], which makes circuit simulation unnecessary. In [5], a moment-based delay analysis method called D2M is applied to simplified circuits, achieving 2500x and 600x speed up for single-fanout paths and multiple-fanout paths. However, the accuracy degradation, especially for multiple-fanout paths, is significant and it is not acceptable.

In this work, we propose a delay model as a function of a few topology parameters that can be immediately obtained instead of RC parameters by exploiting the regular structure of via-switch FPGA and pre-characterization with circuit simulator. The proposed model does not require equivalent circuit construction with RC extraction or circuit simulation when analyzing delay for actual wiring

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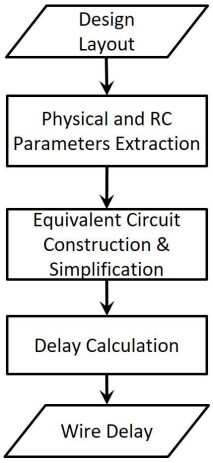

Fig. 1 Equivalent Circuit Construction and Simplication

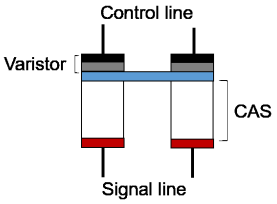

Fig. 2 2V-1CAS via-switch.

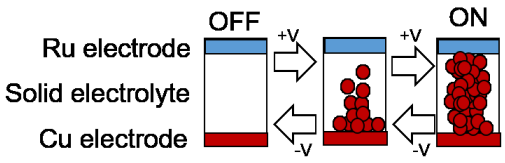

Fig. 3 Atom switch.

patterns. This work focuses on and selects the number of on-state via-switches existing on the path of interest as a key parameter since the resistance of the path is dominated by the on-state via-switches. We also introduce a parameter that expresses the distance difference between x- and y-directions for taking into account rectangular, i.e. non-square, crossbar structure. We experimentally demonstrate that the proposed model can estimate wiring delay accurately for single-fanout and two-fanout interconnects.

The rest of this paper is organized as follows. Section 2 briefly describes the structure of via-switch FPGA. In Section 3, we identify key parameters that should be adopted in the delay functions in single-fanout and multiple-fanout interconnects and present the proposed model. Experimental results are shown in Section 4, and conclusions are drawn in Section 5.

2. Via-Switch FPGA

2.1 Via-switch

Via-switch is a non-volatile, rewritable and compact switch, which was developed to implement a crossbar [8], and it is composed of two varistors and one comlementary atom switch (2V-1CAS). Fig. 2 shows the structure of a 2V-1CAS via-switch. We can find that varistors are connected to the control terminal of the CAS. The two control lines provide reliable one-to-one programming of each cross point without access transistors. Also, this 2V-1CAS structure supports multiple fanouts [3]. When we apply a higher voltage than a threshold value to a set of signal line and control line, programming current is provided to an atom switch of interest through a varistor.

Fig. 3 shows the structure and programming mechanism of an atom switch. The atom switch has a solid electrolyte filled between a copper (Cu) electrode and a ruthenium (Ru) electrode. When a positive voltage is applied to the Cu electrode, Cu ions are generated from the Cu electrode, and a crosslink is formed between the both electrodes. Conversely, when a negative voltage is applied to the Cu electrode, the Cu ions return to the Cu electrode, and the formed crosslink disappears [9,10]. The formation and disappearance of the crosslinks can be repeated.

2.2 Via-switch FPGA structure

In the via-switch FPGA, Configurable Logic Block (CLB) is a basic component, and it is placed in an array as shown in Fig. 4 . Each CLB consists of a logic block (LB) and a crossbar where via-switches are arranged at the intersections of vertical and horizontal wires. LB consists of a look-up table (LUT: Look-Up Table) and a flip-flop (FF: Flip Flop). LB may also include an arithmetic unit or SRAM. The via-switches at the intersections of the crossbar connect or disconnect the vertical and horizontal signal lines. The regions surrounded by the blue line and the yellow line correspond to connection block (CB) and switch block (SB) of the conventional FPGA, respectively. In the via-switch FPGA, the crossbar reconfiguration is performed separately for each CLB, and via-switches also exist between each CLB and adjacent CLBs, which are called inter-CLB via-switches.

There is a signal path drawn in red line in Fig. 4 as an example. Each small red square represents an on-state via-switch. The path starts from the LB in the top left CLB and end at the LB in the bottom right CLB crossing through two CLBs. On this signal path, there are six on-state via-switched in total, where four via-switches inside CLBs and two inter-CLB via-switches are included.

In the following, we assume the following specifications of via-switch FPGA.

- Chip manufacturing: 65nm process
- Crossbar size: 163×69

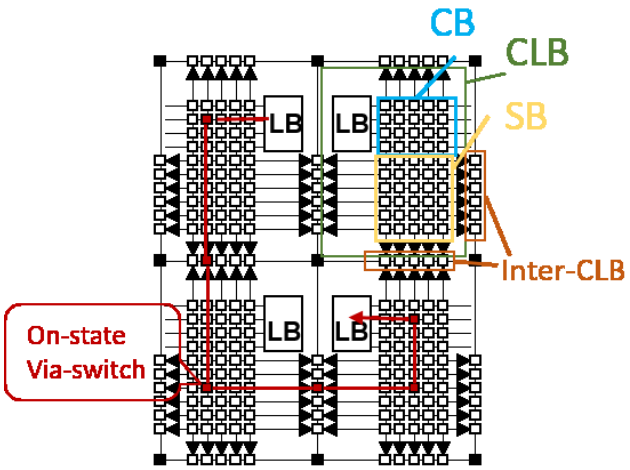

Fig. 4 Structure of via-switch FPGA

- Driver resistance: 1kΩ
- Via-switch resistance: 400 Ω (ON) / 400 MΩ (OFF)
- Other signals: grounded

3. Proposed Delay Model

This section discusses a wiring delay model that requires no RC extraction and instead focuses on the number of on-state via-switches. In the via-switch FPGA, we observe that the resistance of on-state via-switch, which is 400Ω as shown in the previous section, is larger than wire metal resistance. Therefore, we suppose the number of on-state via-switches plays an important role in wiring delay analysis. Hereafter, we separately discuss the delay model in single- and two-fanout cases.

3.1 Single Fanout

As mentioned above, we focus on the number of on-state via-switches in the path of interest since it mostly contributes to the total resistance. Also, the wire length is roughly proportional to the number of on-state via-switches since at least one inter-CLB via-switch is added per every CLB.

We quantitatively evaluate the relation between the wiring delay DT_{FO1}, which is obtained with an equivalent circuit model and circuit simulation referring to [5], and the number of on-state via-switches N. For this evaluation, we generated 1,200 wiring patterns randomly. The relationship between N and DT_{FO1} is shown in Fig. 5. We can see that there is a clear relation between N and DT_{FO1}. When we fit the relation into a second-order polynomial expression, the coefficient of determination (R^2) attains 0.996. N is the dominant factor for wiring delay model as we expected, and we conclude DT_{FO1} can be expressed as a function of N.

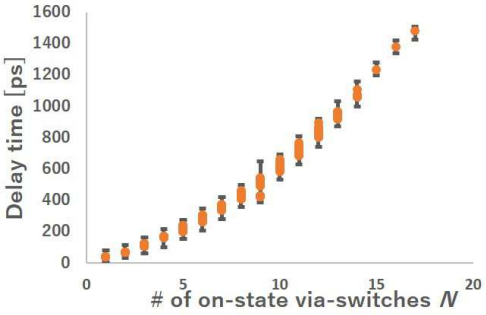

Fig. 5 Relation between wiring delay and N for single-fanout wires.

$$DT_{FO1} = f_N^{(1)}(N). \quad (1)$$

On the other hand, we notice that there remains uncertainty in delay time originating from the wiring topology. We guess that this uncertainty comes from the uneven crossbar size in x- and y-directions, i.e., the horizontal and vertical lengths, which are proportional to the number of via-switches, are different as shown in the previous section, even when N is the same. In case that the path goes vertically, the path becomes longer and the delay is expected to be larger compared to the horizontal case. For confirming this guess, we constructed two paths for each N value; one is the path consisting of as many vertical wire segments as possible (VER), and the other is the path consisting of as many horizontal wire segments as possible (HOR).

Table 1 shows the delay difference between VER and HOR. For comparison, we also show the maximum and minimum delay times and their difference for the randomly-generated samples in Fig. 5. We can see that the difference in the randomly-generated samples can be mostly explained by the difference between VER and HOR. For mitigating the uncertainty in Eq. (1), we should consider the topological direction. Here, note that the remaining difference that cannot be explained by the difference between VER and HOR is supposed to originate from the location of on-state via-switch inside the crossbar, etc. We thus redefine the wiring delay model as follows:

$$DT_{FO1} = f_{ND}^{(1)}(N, D_{v-h}), \quad (2)$$

where D_{v-h} is the distance difference between the horizontal and vertical directions. The detailed and appropriate definition of D_{v-h} will be experimentally evaluated in Section 4.

The function $f_{ND}^{(1)}(N, D_{v-h})$ can be prepared as a look-up table (LUT) or a closed-form expression. In both cases, the wire delay can be computed immediately for any single-fanout wires without equivalent circuit construction or circuit simulation. Besides, when we derive a closed-form expression via regression, we need to carefully determine

Table 1 Comparisons between randomly generated topologies and VER and HOR paths in single-fanout case.

N	Topologies	Delay [ps]		Difference
		Max	Min	[ps]
9	VER&HOR	552	504	48
	Random	560	504	55
10	VER&HOR	661	597	64
	Random	661	596	64
11	VER&HOR	780	701	80
	Random	779	684	95

the expression to be fitted. Here, we refer to Elmore delay model. For this discussion, we assume

$$\begin{aligned} R &= \alpha_1 N + \beta_1 D_{v-h} + \gamma_1 \\ C &= \alpha_2 N + \beta_2 D_{v-h} + \gamma_2 \end{aligned} \tag{3}$$

where $\alpha_1, \beta_1, \gamma_1 \alpha_2, \beta_2$ and γ_2 are constants. R is the total resistance of path, and C is the total capacitance of the path. An off-state via-switch is regarded as a capacitance and the metal capacitance is proportional to the length. Therefore, C is also expected to be proportional to N. Taking into account the Elmore delay expression, we fit the following second-order polynomial expressions to the corresponding circuit simulation results.

$$f_N^{(1)}(N) = aN^2 + bN + c, \tag{4}$$

$$f_{ND}^{(1)}(N, D_{v-h}) = a'N^2 + b'N + c'D_{v-h}^2 + e'D_{v-h} + f'. \tag{5}$$

where a, b, c and a', b', c', d', e', f' are constants, and they are determined by regression with a set of pre-characterized simulation results.

3.2 Two Fanout

Next, we build wiring delay models for two-fanout paths that have one source and two sinks. A two-fanout path is divided into three parts at a junction shown in Fig. 6, and we extract the numbers of on-state via-switches from every part as N_1, N_2, N_3, where N_1 is the number of via-switches in the common path, N_2 is that in the non-common path to the target sink, and N_3 is that in the branch path.

Here, A two-fanout path can be transformed to a RC tree. The Elmore delay for the path from the source to the target sink, which is depicted in blue Fig. 6, is given by

$$DT_{Elmore} = R_1(C_1 + C_2 + C_3) + R_2C_2, \tag{6}$$

where R_1 and R_2 are the resistances of the path segments corresponding to N_1 and N_2, and C_1, C_2, and C_3 are the capacitances corresponding to N_1, N_2 and N_3, respectively. We can suppose R_1, and R_2 are proportional to N_1 and N_2, respectively, as Eq. (3). C_1, C_2, and C_3 are similar. We thus adopt the following expression for regression.

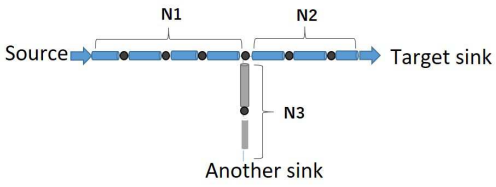

Fig. 6 A two-fanout path with three segments and the number of on-state via-switches for each segment.

$$\begin{aligned} DT_{FO2} &= f_N^{(2)}(N_1, N_2, N_3) \\ &= aN_1^2 + bN_1N_2 + cN_1N_3 + dN_2^2 \\ &\quad + eN_1 + fN_2 + gN_3 + h \end{aligned} \tag{7}$$

where a, b, c, d, e, f, g, h are constants determined by regression.

On the other hand, similar to the single-fanout case, there is delay uncertainty even N_1, N_2, N_3 are specified. Table 2 shows three examples of (9, 9, 9) to (11, 11, 11). For each set, samples are randomly generated and evaluated. For confirming that this uncertainty comes from the distance difference in the vertical and horizontal directions, we also evaluated the delay times of vertical (VER) and horizontal (HOR) paths. We can see that the difference between VER and HOR paths is larger than the maximum difference observed in the random samples because the number of evaluated samples is not large enough. On one hand, this result indicates that the distance difference between vertical and horizontal directions has a big impact on wiring delay analysis behind the number of via-switches (N_1, N_2, N_3).

Therefore, we should add a few new parameters that can represent the vertical and horizontal distance difference to the delay model. When we prepare the delay model using LUT, the number of additional parameters should be minimized even while two-fanout paths consist of three segments as shown in Fig. 6. Our goal is to achieve a simple function to estimate wiring delay, and then we try to find a good definition of a single representative parameter. For this purpose, we adopt D_m as a new parameter, which stands for the vertical and horizontal distance difference on the main path, i.e. the path between the source and target sink.

$$\begin{aligned} DT_{FO2} &= f_{ND}^{(2)}(N_1, N_2, N_3, D_m) \\ &= aN_1^2 + bN_1N_2 + cN_1N_3 + dN_2^2 + eN1 + fN2 + gN3 \\ &\quad + hD_m^2 + iD_m + j, \end{aligned} \tag{8}$$

where $a, b, c, d, e, f, g, h, i, j$ are constants.

Table 2 Comparisons between randomly generated topologies and VER and HOR paths in two-fanout case.

N_1, N_2, N_3	Topologies	Delay [ps]		Difference
		Max	Min	[ps]
9, 9, 9	VER&HOR	2747	2387	360
	Random	2621	2377	244
10, 10, 10	VER&HOR	3371	2891	480
	Random	3076	2863	213
11, 11, 11	VER&HOR	4049	3452	597
	Random	3741	3401	340

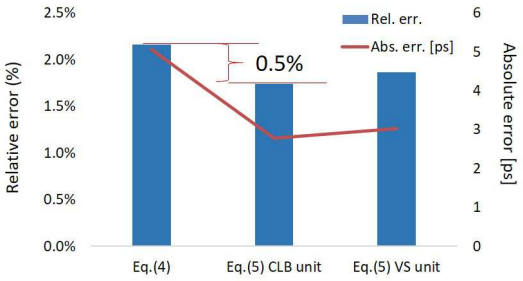

Fig. 7 Estimation error comparison with different regression functions (single-fanout case).

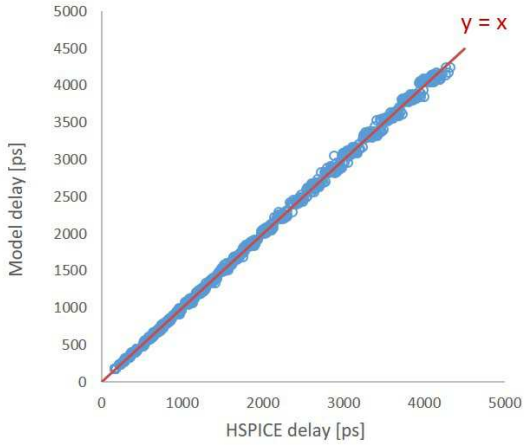

Fig. 8 Delay comparison between the proposed model and HSPICE (single-fanout case).

4. Experimental Results

This section evaluates the accuracy of the proposed model. The crossbar size, via-switch and driver resistance are the same as described in Section 2.

4.1 Single Fanout

We make 1300 single-fanout paths randomly for accuracy evaluation, where the total number of on-state via-switches included the paths is less than 30 ($N < 30$). For each path, we construct an equivalent circuit model referring to [5] and simulate it with HSPICE. Then, we use the delay times obtained by HSPICE to determine the coefficients in Eq. (1) with MATLAB. Here, we use the following two definitions of D_{v-h} in Eq. (5).

- counting the distance in CLB unit,
- counting the distance in via-switch unit.

The CLB unit is suitable for LUT implementation since the value range is not large while the via-switch unit might provide better accuracy.

The accuracy evaluation results are shown in Fig. 7. When Eq. (5), which does not include D_{v-h}, is used, the averages of absolute and relative errors are 5.1ps and 2.2%, respectively. On the other hand, with D_{v-h} in CLB and via-switch units, the relative errors are reduced to 1.7% and 1.9%, respectively. The absolute errors are similarly reduced. On the other hand, the difference originating from the unit difference in D_{v-h} is small, and the courser unit of CLB achieves smaller estimation error. Therefore, the CLB unit is suitable for D_{v-h}.

Fig. 8 shows a scatter plot between the HSPICE result and the proposed model of Eq. (5) with CLB unit. We confirm there are no outlines.

4.2 Two Fanout

We next evaluate two-fanout paths. We randomly generated 4780 two-fanout paths. Each path has less than 30 on-state via-switches in total, i.e. $N_1 + N_2 + N_3 < 30$, and N_1, N_2 and N_3 are more than 4 and less than 22.

Fig. 9 shows the averages of relative and absolute errors for Eq. (7) and Eq. (8) with CLB and via-switch units. The averages of absolute and relative errors for Eq. (7) are 205ps and 4.3%. When the distance difference in vertical and horizontal directions are considered with Eq. (8), the errors are reduced. With CLB unit, the absolute and relative errors are 27ps and 1.8%, which is much smaller than those of Eq. (7), and the absolute error is especially reduced by 87%. On the other hand, when the via-switch unit is used, the absolute relative error increases to 51ps compared to the CLB unit case. Therefore, the CLB unit is suitable for the proposed model similar to the single-fanout case.

Fig. 10 shows the scatter plot between HSPICE delay and Eq. (8) with CLB unit. We can see there are no outliners while the variation is larger than that of the single-fanout case in Fig. 8.

5. Conclusion

This paper has proposed an interconnect delay model for via-switch FPGA that mainly focuses on the number of on-state switches and distance difference in vertical and hori-

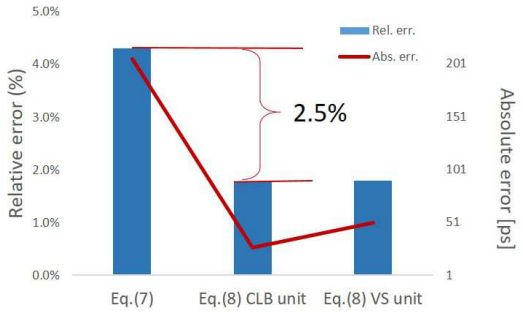

Fig. 9 Estimation error comparison with different regression functions (two-fanout case).

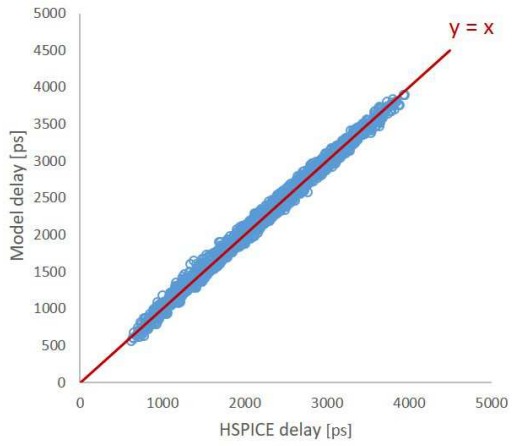

Fig. 10 Delay comparison between the proposed model and HSPICE (two-fanout case).

zontal directions. We construct model expressions through regression with pre-characterized circuit simulation results, and consequently we can compute wiring delay without RC extraction or circuit simulation for actual wire patterns. Experimental results for 1300 single-fanout paths show that the estimation error is within 1.7% on average. As for 4780 two-fanout paths, the relative average error is 1.8%. Our future work includes the model extension to larger-fanout paths while preserving the simple expressions.

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