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【基調講演】

Challenges towards HLS Optimization in Modern FPGA

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Modern FPGAs have been facilitating with remarkable features such as embedded multi-core CPU, floating-point co-processors, high-speed connectivity, storage and signal processing blocks. More and more complicated applications require high speed for fast system response. However, there are still some limitations such as resources, bus systems, operating systems, and design tools. Therefore, HLS (High-Level Synthesis) optimization is needed to maximize the performance of FPGAs under speed, power, and resource constraints. Here, potential HLS optimization techniques are reviewed. Finally, challenges towards HLS optimization in modern FPGA are raised in terms of memory management, bus management, task scheduling, data flow architecture, and clocking.

1. Current Career

Head of Department, Department of Electrical Engineering, Faculty of Engineering, Prince of Songkla University, 2016 –

2. Educations

March 1993:	B.Eng. (Electrical), Prince of Songkla University, Thailand
October 2000:	M.Eng. (Information), The University of Tokyo, Japan
March 2004	Ph.D. (Interdisciplinary Course on Advanced Science and Technology), The University of Tokyo, Japan

3. Field(s) of Specialization

Digital Very Large Scale Integrated (VLSI) circuit design: High-Level Synthesis (HLS)
Embedded systems and Field Programmable Gate Array (FPGA) applications
Wireless sensor networks
Electrostatic Discharge (ESD)
Model Based Design

4. Current Research Areas/Topics:

High-Level Synthesis (HLS)
Field Programmable Gate Array (FPGA) applications
V2V communications
Model Based Design

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