Implementation of ROS-Compliant FPGA Component of Image Processing Hardware using High Level Synthesis

Yuhei Sugata[†1] Takeshi Ohkawa[†1] Kanemitsu Ootsu[†1] Takashi Yokota[†1]

Abstract: The advancement of intelligents robot require high-performance image processing with low power consumption. FPGA (Field Programmable Gate Array) is expected to perform this image processing with low power consumption, however, the cost of developing FPGA is too high to introduce. To reduce the development cost, High Level Synthesis (HLS), which generates hardwired circuits from behavioral description written by C language, is effective. On the other hand, the use of ROS (Robot Operating System) is increasing for the development of intelligent robot system in order to reduce the development. We proposed "ROS-Compliant FPGA Component" to introduce FPGA into robot easily, by componentizing FPGA circuit into ROS node. In this presentation, the implementation of the ROS-Compliant FPGA component of image processing hardware using HLS is described. As an example, a detailed implementation of ROS-Compliant FPGA component with FAST feature point detection circuit, which is generated by using Xilinx Vivado-HLS and HLS video library based on OpenCV, is explained.

Keywords: FPGA, ROS, Robot, High Level Synthesis, Image Processing

†1 Graduate School of Engineering, Utsunomiya University