32-09

Optimal Layouts of Virtual Paths in Complete Binary Tree ATM Networks *

Suguru Amitani, Toshinori Yamada, and Shuichi Ueno †
Dept. of Communications and Integrated Systems,
Graduate School of Science and Engineering, Tokyo Institute of Technology,
Tokyo 152-8552, Japan
{ amitani, yamada, ueno } @ss.titech.ac.jp ‡

1 Introduction

The ATM(Asynchronous Transfer Mode) is well-known as a multiplexing and switching technology for multipurpose broadband high-speed networks. We follow a mathematical model of ATM networks which was introduced by Cidon, Gerstel, and Zaks [CGZ94], and further developed by Kranakis, Krizanc, and Pelc [KKP95]. In an ATM network, pairs of nodes exchange messages along pre-defined paths, called virtual paths. Each connection between two nodes must consist of a concatenation of such virtual paths. The layout is a collection of virtual paths that guarantees the connection for every pair of nodes. The hop number of a layout is the maximum, taken over all pairs of nodes, of the smallest number of virtual paths used to connect a pair of nodes. The congestion of a layout is the maximum number of virtual paths that pass through a link. The hop number corresponds to the time to set up a connection between a pair of nodes, and the congestion measures the load of the routing tables at the nodes.

It is a fundamental problem to construct a layout minimizing the hop number as a function of the congestion. For a network G, $\mathcal{H}_G(c)$ is the minimum hop number over all layouts with congestion at most c. Kranakis, Krizanc, and Pelc [KKP95] showed a general lower bound for $\mathcal{H}_G(c)$. They proved that for any N-node network G with maximum node degree Δ, and for any positive integer c, $\mathcal{H}_G(c) \geq \log N/\log(c\Delta) - 1$. On the other hand, Stacho and Vrťo [SV00] showed a general layout with hop number $O(\mathrm{diam}(G)\log\Delta/\log c)$, where $\mathrm{diam}(G)$ is the diameter of G. It follows that if $\Delta = O(1)$ and $\mathrm{diam}(G) = O(\log N)$ then $\mathcal{H}_G(c) = \Theta(\log N/\log c)$ for any c. In particular, we have asymptotically optimal bounds for $\mathcal{H}_G(c)$ if G is a mesh of trees, butterfly, cube-connected-cycles, de Bruijn network, shuffle-exchange network, or complete binary tree network. However, there is a considerable gap between the upper and lower bounds above.

The purpose of the paper is to close the gap for complete binary tree networks. We show the exact value of minimum hop number for complete binary tree networks. Our results are presented in the following theorem.

Theorem 1 *For an N-node complete binary tree network B_N with height L and a positive interger c,*

$$\mathcal{H}_{B_N}(c) = \begin{cases} 1 & \text{if } 1 \leq L \leq \left\lfloor \log\left(1+\sqrt{1+4c}\right)\right\rfloor - 1, \\ 2 & \text{if } \left\lfloor \log\left(1+\sqrt{1+4c}\right)\right\rfloor \leq L \leq \lfloor \log(c+1)\rfloor, \\ 3 + \left\lceil \frac{2L - 2\lfloor\log(c+1)\rfloor - \lceil \log c\rceil - 1}{\lfloor \log c\rfloor + 1}\right\rceil & \text{otherwise,} \end{cases}$$

where $L = \log(N+1) - 1$. □

---

*完全二分木 ATM ネットワークにおける最適な仮想パスレイアウト

†網谷 優, 山田 敏規, 上野 修一
‡東京工業大学大学院 理工学研究科 集積システム専攻

Theorem 1 is proved by showing tight upper and lower bounds. We just show layouts and give a sketch of the proof for upper bounds.

2 Layouts

Case 1. $1 \le L \le \lfloor \log(1+\sqrt{1+4c}) \rfloor - 1$: The layout is the set of paths connecting every pair of distinct vertices. It is easy to see that the congestion of the layout is c, and the minimum hop number is 1.

Case 2. $\lfloor \log(1+\sqrt{1+4c}) \rfloor \le L \le \lfloor \log(c+1) \rfloor$: The layout is the set of paths connecting the root of the tree and all the other vertices. It is easy to see that the congestion of the layout is c, and the minimum hop number is 2.

Case 3. $L \ge \lfloor \log(c+1)+1 \rfloor$: Let m be the integer satisfying $L = \lfloor \log(c+1) \rfloor + m(\lfloor \log c \rfloor + 1) + x$, where $0 \le x \le \lfloor \log c \rfloor$. Let $\mathcal{P}$ be the set of paths connecting each vertex v on level $L - \lfloor \log(c+1) \rfloor$ and the descendants of v. For $0 \le i \le m$, let $\mathcal{Q}_i$ be the set of paths connecting each vertex v on level $L - \lfloor \log(c+1) \rfloor - i(\lfloor \log c \rfloor + 1)$ and the ancestors of v on levels l for $L - \lfloor \log(c+1) \rfloor - (i+1)(\lfloor \log c \rfloor + 1) \le l \le L - \lfloor \log(c+1) \rfloor - i(\lfloor \log c \rfloor + 1) - 1$.

Subcase 3-1. $x = 0$: The layout is $\bigcup_{i=1}^{m-1} \mathcal{Q}_i \cup \mathcal{P}$.

Subcase 3-2. $1 \le x \le (\lceil \log c \rceil + 1)/2$: Let $\mathcal{R}$ be the set of two paths connecting the root r and two children s, t of r, $\mathcal{A}$ be the set of paths connecting each vertex v on level x and the ancestors of v except r, and $\mathcal{B}$ be the set of paths connecting each descendant of s on level x and each descendant of t on level x. The layout is $\bigcup_{i=1}^{m-1} \mathcal{Q}_i \cup \mathcal{P} \cup \mathcal{R} \cup \mathcal{A} \cup \mathcal{B}$.

Subcase 3-3. $(\lceil \log c \rceil + 1)/2 < x \le \lfloor \log c \rfloor$: The layout is $\bigcup_{i=1}^{m} \mathcal{Q}_i \cup \mathcal{P}$.

It can be proved that for any subcase, the congestion of the layout is c, and the minimum hop number is $3 + \lceil (2L - 2\lfloor \log(c+1) \rfloor - \lceil \log c \rceil - 1)/(\lfloor \log c \rfloor + 1) \rceil$.

3 Generalization

Theorem 1 can be generalized to complete k-ary tree networks as follows.

Theorem 2 *For an N-node complete k-ary tree network $T_{k,N}$ with height L and a positive interger c,*

$$\mathcal{H}_{T_{k,N}}(c) = \begin{cases} 1 & \text{if } 1 \le L \le \left\lfloor \log_k \left(1+\sqrt{1+4c(k-1)}\right) - \log_k 2 \right\rfloor, \\ 2 & \text{if } \left\lfloor \log_k \left(1+\sqrt{1+4c(k-1)}\right) - \log_k 2 \right\rfloor + 1 \le L \le \lfloor \log_k (c+1) \rfloor, \\ 3 + \left\lceil \frac{2L - 2\lfloor \log_k (c+1) \rfloor - \lceil \log_k \frac{c}{k-1} \rceil - 1}{\lfloor \log_k c \rfloor + 1} \right\rceil & \text{otherwise,} \end{cases}$$

where $L = \log_k((k-1)N+1) - 1$. □

Acknowledgments: The authors are grateful to Prof. Y. Kajitani for his encouragement. The research is a part of CAD21 Project at TIT.

References

[1] Ladislav Stacho and Imrich Vrťo, "Virtual Path Layouts in ATM Networks", SIAM J. Comput. Vol. 29, No. 5, pp. 1621-1629(2000)

[2] E.Kranakis,D.Krizanc and A.Pelc, "Hop-Congestion Trade-Offs for High-Speed Networks", Proc. 7th IEEE Symposium on Parallel and Distributed Processing,pp.662-668(1995).