LC-004

Feasibility of Interconnect Open Detection by Ramp Voltage Application

Yukiya Miura †

1. Introduction

Interconnect open faults often occur because present deep-submicron VLSIs are fabricated by using copper process technologies and multiple metal layers [1]-[3]. The VLSI circuit with an open fault shows various complicated fault behaviors such as low noise margins, signal integrity problems, performance degradation, and so on.

Application of logic testing (e.g., stuck-at faults testing) is reported to detect open faults [4]-[6]. Especially, it is said that *n*-detection testing is useful for detecting open faults [7]. However, voltages of signal lines around the fault location depend on applied test vectors, and the voltage at the fault location depends on the balance of wire capacitances between the VDD side and the GND side. Therefore, it is difficult to detect open faults surly by logic testing even if we use *n*-detection testing [8].

If a known logic value can be compulsorily set to the fault location, fault detection by logic testing can be realized easily. Based on this motivation, we have proposed a method for detecting interconnect open faults by applying ramp voltage to power supply terminals, where an initial logic value at a fault location is automatically assigned when the ramp voltage is applied [9]. The method requires only one test vector and the fault is detected as a delay fault or an erroneous logic value at primary outputs.

In this paper, we show ability and effectiveness of our testing method. We show fault detectability of the proposed method by using simulation and theoretical analysis. We also expose that the method is applicable for detecting interconnect open faults with unknown value. Moreover, we show ATPG results that are suitable to our testing method, where test generation is done so that the number of lines assigned logical values by a test vector is smaller as much as possible.

This paper is organized as follows. Section 2 describes a method for detecting interconnect open faults. Section 3 shows effectiveness of the proposed method by using simulation results and theoretical analysis. Besides, we show results of ATPG that is suitable to the proposed method. Section 4 concludes the paper.

2. Principle of interconnect open fault detection [9]

In this paper, we consider only interconnect open faults between two gates as shown in Fig. 1. In general, interconnect open faults are modeled by a RC circuit [10], [11], where Rf is an open resistance and Cw1 (Cw2) is a total wire capacitance between the signal line having an open fault and signal lines having the VDD (VSS) voltage.

The difficultness of open fault detection by logic testing comes from assignment of a known voltage (a known logic value) to the open fault location. In order to improve the difficulty, we have proposed the following testing method (Fig. 2).

(1) All input terminals including power supply terminals of the circuit are set to the GND level at time 0 [t0]. Then, all internal nodes in the circuit are also set to the GND level.
(2) A positive ramp voltage with a certain slope is applied to the VDD terminal during the interval [t1, t2]. Note that logic 0 is automatically assigned to the fault location.
(3) After the node voltage fully settles down [t3], apply one test vector to change the logic value at the open fault location, propagate it to the primary output, and observe an output value at a predetermined time [t4].
(4) If the output value does not change within a specific time interval, we judge there is an open fault and finally, we can detect the fault [t4]. In Fig. 2, this fault causes the delay time of tpd.

In the above procedure, if we apply a negative ramp voltage to the VSS terminal in the above Step (2), the initial value is logic 1 and logic 0 for the testing interval. Therefore, our testing method can set both logic values as the initial value.

Since the equivalent circuit of Fig. 1 is represented by the RC differential circuit of Fig. 3 when N1=VSS=GND and VDD=(positive voltage), the voltage of the N2 node, V_{N2}, is expressed as follows if a ramp voltage is applied:

$$V_{N2}(t) = k \cdot Cw1 \cdot Rf \cdot (1 - e^{-\frac{t}{Rf(Cw1+Cw2)}}) , \quad (1)$$

where Vi(t)=*k*t (ramp voltage) and Vi(0)=0. This equation

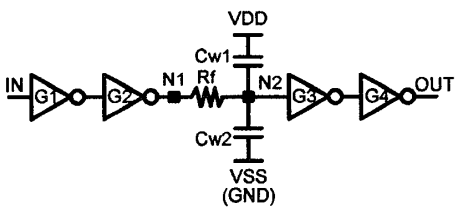

Fig. 1 Circuit and fault models.

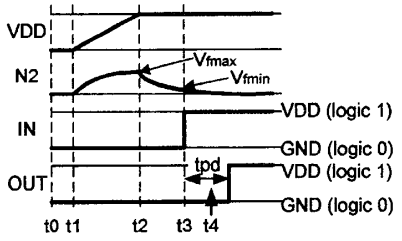

Fig. 2 Testing method of VDD application.

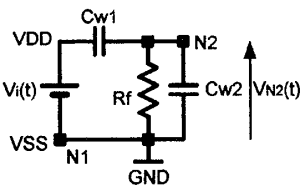

Fig. 3 Equivalent circuit.

† Graduate School of Engineering, Tokyo Metropolitan University

Table 1 Results of circuit simulation and theoretical analysis.

			Simulation			Theory w/o CL			Theory with CL		
Sim. No.	Test & Circuit types	Rf, Cw1,Cw2 [MΩ] [fF]	Vfmax [mV]	Vfmin [mV]	tpd [μs]	Vfmax [mV]	Vfmin [mV]	tpd [μs]	Vfmax [mV]	Vfmin [mV]	tpd [μs]
S1	Typical gates VDD application	100, 80, 8	698.9	90.2	6.76	645.8	66.5	6.10	686.5	89.6	6.81
		100, 8, 8	146.0	0.042	2.05	72.0	0.0	1.11	141.5	0.069	1.82
		100, 8, 80	127.1	16.2	6.72	64.6	6.7	6.10	123.1	16.1	6.81
S2	G2=typ, G3=5*typical VDD application	100, 80, 8	816.2	182.4	8.91	645.8	66.5	6.10	788.7	172.9	9.13
		100, 8, 8	375.3	11.4	5.53	72.0	0.0	1.11	349.4	12.3	4.14
		100, 8, 80	299.9	63.8	9.91	64.6	6.7	6.10	282.8	62.0	9.13
S3	G2=typ, G3=10*typical VDD application	100, 80, 8	879.8	304.4	11.26	645.8	66.5	6.10	876.3	275.5	11.98
		100, 8, 8	577.8	74.2	8.87	72.0	0.0	1.11	543.4	74.8	6.99
		100, 8, 80	458.9	140.1	12.88	64.6	6.7	6.10	432.0	135.8	11.98
S4	Typical gates VDD application	100k, 80, 8	0.80	0.0	6.87n	0.72	0.0	6.10n	0.79	0.0	6.81n
		100k, 8, 8	0.15	0.0	1.70n	0.072	0.0	1.11n	0.14	0.0	1.82n
		100k, 8, 80	0.15	0.0	7.04n	0.072	0.0	6.10n	0.14	0.0	6.81n
S5	Typical gates VDD application	1k, 80, 8	13.43u	0.0	0.64n	7.20u	0.0	0.061n	7.90u	0.0	0.068n
		1k, 8, 8	2.75u	0.0	0.34n	0.72u	0.0	0.011n	1.42u	0.0	0.018n
		1k, 8, 80	2.75u	0.0	0.64n	0.72u	0.0	0.061n	1.42u	0.0	0.068n

gives V_{N2} for the interval [t1, t2].
If the initial voltage of $V_i(0)$ is V_0, the V_{N2} voltage is given as follows:

$$V_{N2}(t) = \frac{Cw1}{Cw1+Cw2} \cdot V_0 \cdot e^{-\frac{t}{Rf(Cw1+Cw2)}} \quad . \qquad (2)$$

Note that considering our testing procedure, coefficient (Cw1/(Cw1+Cw2))V_0 of the right-hand side of Eq. (2) results in $V_{N2}(t2)$ obtained from Eq. (1) because $V_{N2}(t)$ at t2 is given by Eq. (1) when t=t2. Then, V_{N2} is given by Eq. (2) for the interval [t2, t3].

The equivalent circuit of VDD (VSS) application for faults at even inversion gates corresponds to one of VSS (VDD) application for faults at odd inversion gates. Therefore, the proposed method is applicable to open faults at every location of CMOS combinational circuits.

Since the voltage stability of the fault location depends on both the balance between Cw1 and Cw2 and the positive/negative of the applying power supply voltage, we have to examine two methods, VDD application and VSS application, for each location. Especially, if Cw1<Cw2 (Cw1>Cw2), the positive (negative) power supply application is better (see Table 1).

3. Effectiveness of open fault detection method

In order to show the effectiveness of the proposed method, we carry out circuit simulation by using the circuit of Fig. 1 and the TSMC-0.18μm technology [12]. Simulation conditions are as follows: (VDD ramp voltage)=1.8V/20μsec, Rf=1kΩ~100MΩ, {Cw1, Cw2}= {8fF, 80fF}, L=0.18μm, (Wp/Wn of the typical gate)= 3.3μm/1.0μm

3.1 Theoretical analysis of interconnect open faults

In this section, we consider electrical behaviors of the open fault by Eqs. (1) and (2) (i.e., theoretical analysis). We evaluate voltages of the open fault location, Vfmax and Vfmin, and the delay time for fault detection, tpd (see Fig. 2).

Table 1 shows simulation results and theoretical analysis results for several fault values. Simulations S2 and S3 are results of driven gate G3 whose sizes are 5*Wp/Wn and 10*Wp/Wn, respectively.

Results of Vfmax and Vfmin by theoretical analysis ("Theory w/o CL" column) have a few differences compared with those of simulations. Especially, there is a large difference between simulation results and theoretical analysis as the size of the driven gate G3 is larger. This is explained as follows. If load capacitances of the driven gate have an enough impact for wire capacitances at the fault location, their effects appear for the voltage at the fault location and the delay time at the primary output. In the rest of paper, we take the load capacitance of the driven gate into account in theoretical circuit analysis. Since a faulty circuit can be modeled by the RC circuit of Fig. 3, wire capacitances of Cw1 and Cw2 can be rewritten as follows:

Cw1 ← Cw1+CLp, Cw2 ← Cw2+CLn

Here, the load capacitance of a transistor consists of the diffusion capacitance and the gate capacitance whose values depend on a transistor's operation. For the simple discussion, we consider worst values of load capacitances; for instance, CLp=7.73fF and CLn=2.50fF for the typical gate size. Therefore, theoretical V_{N2} values show worst values compared with those of simulation results (i.e., actual values are within the safety side). As shown in the column of "Theory with CL" of Table 1, results of the theoretical analysis considering the load capacitance agree well with those of the SPICE simulation, where their average differences are within 3.3% for Vfmax and Vfmin.

From results of Table 1, by using our testing method, we find that the delay time by a fault is proportion in the time constant because the interconnect open fault is modeled by the RC difference circuit and its time constant is Rf(Cw1+Cw2). Then, in the theoretical analysis by the RC difference circuit, we can say that the delay time is proportion in the time to reach the voltage of 50% of VDD at the fault location. Then, we can estimate that delay time is 0.69τ where the fault has the time constant τ. The tpd column of "Theory with CL" in Table 1 shows calculation results, where those values are almost consistent with simulation results (Their differences are within 8.4%).

3.2 Application to open faults with unknown value

In this section, we show that our method can apply to open faults with unknown value (i.e., open faults with RC value of wide range).

According to Eq. (1), the N2 voltage is mainly in proportion to both k and Cw1Rf. Therefore, since the N2 voltage is easy to rise as Cw1Rf becomes larger, to prevent the voltage rising of N2, it is necessary to apply a ramp voltage with a small k (i.e., a ramp voltage with a gentle slope). If we can determine (or assume) the maximum value of Cw1Rf to be detected in advance, we can set the slope k to prevent voltage rising at the fault location. Therefore, determination of k (the slope of the ramp voltage) depends on the maximum value of the open fault to be detected/assumed.

For instance, if we assume that Vfmax is almost the same even if an RC value is changed, we can calculate the slope k of a fault with (Rf, Cw1, Cw2) for the given standard values (k_0, t_0, Rf_0, $Cw1_0$, $Cw2_0$) as follows:

$$k = \frac{m \cdot n}{m+n} \quad , \tag{3}$$

$$m = \frac{Cw1_0 \cdot Rf_0 \cdot (1 - e^{-\frac{t_0}{Rf_0(Cw1_0+Cw2_0)}})}{Cw1 + Rf} \cdot k_0 \quad , \tag{4}$$

$$n = -\frac{VDD}{Rf(Cw1+Cw2)} \quad . \tag{5}$$

Table 2 shows those calculation and simulation results for the standard Vfmax (indicated by *), where we can obtain almost the same Vfmax value for several parameters. Note that calculation results obtained from the above equations give approximate estimates because Eq. (1) represents the response of the equivalent circuit and load capacitances of the driven gate vary with transistor's operation. Moreover, since the value of the *exp* function of Eq. (1) becomes larger as the Cw2 value becomes larger, Vfmax becomes smaller. Then, we can set the VN2 value to a safety side.

Table 2 Calculation of ramp voltage slope.

			Simulation		Theory	
	Rf, Cw1,Cw2 [MΩ] [fF]	k (slope) [mV/μs]	Vfmax [mV]	Vfmax/VDD [%]	Vfmax [mV]	Vfmax/VDD [%]
*	100, 80, 8	90	698.9	38.8	686.5	38.1
	0.1, 80, 8	78251	653.6	36.1	620.5	34.5
	1, 80, 8	7825	645.6	35.9	620.5	34.5
	10, 80, 8	783	638.3	35.5	620.5	34.5
	100, 80, 40	78	575.3	32.0	569.1	31.6
	100, 80, 80	78	514.0	28.6	508.8	28.3
	100, 8, 8	436	563.5	31.3	544.0	30.2
	100, 8, 40	436	356.4	19.8	348.4	19.4
	100, 8, 80	401	237.9	13.2	231.3	12.9

On the other hand, if a fault value (Rf, Cw1, and Cw2) is small, the delay time by the fault is also small because the time constant of the fault is Rf(Cw1+Cw2). Then, if we wish to detect a fault with a small fault value, we need to set the observation time at the primary output to the minimum estimated delay time caused by an assuming fault and the minimum measurable value by an instrument. Therefore, the observation time at the primary output corresponds to the minimum value of a fault to be detected.

From the above discussion, our testing method can apply to interconnect open faults with values of wide range.

3.3 Test vectors and related phenomena

In the proposed method, the initial logic value at the fault location is automatically assigned when the ramp voltage is applied to the power supply terminal. Then, only one test vector is needed, which has to assign a complementally logical value to the fault location and propagate it to the primary output. Therefore, test generation algorithm and complexity are just the same as those for stuck-at faults. Table 3 shows ATPG results based on the PODEM algorithm where for every circuit, we can obtain the fault efficiency of 100%. Note that *don't care* at primary inputs (unspecified PIs) after generating a test vector remains. The column "PODEM" shows results of the original PODEM algorithm where from the most left column, the number of test vectors, and the average, maximum and minimum numbers of signal lines with specified logical values.

In our testing method, it is desirable that wire capacitances, Cw1 and Cw2, around a fault location are almost constant during the testing interval because the node voltage at the fault location depends on the balance between Cw1 and Cw2. In order to achieve this purpose, the following test generation is appropriate: the number of signal lines where logical values are assigned by a test vector is smaller (i.e., the number of signal lines with *don't care* values is larger as much as possible).

Therefore, we use the following heuristic measurement for the path selection. This means that path selection for the backward/propagation operation is carried out so that the number of signal lines that are assigned logical values by a test vectors is smaller as much as possible. Assume

Table 3 Evaluation of the number of signal lines with specified logical values.

Circuits	PODEM *							Proposed *						
	# Vectors	Ave.		Max.		Min.		# Vectors	Ave.		Max.		Min.	
c432	155	234	54.2%	422	97.7%	49	11.3%	223	150	34.7%	347	80.3%	28	6.5%
c499	125	309	61.9%	499	100.0%	92	18.4%	165	254	50.9%	499	100.0%	55	11.0%
c880	363	398	45.2%	745	84.7%	90	10.2%	512	310	35.2%	627	71.3%	50	5.7%
c1355	204	504	37.2%	1355	100.0%	148	10.9%	304	412	30.4%	1355	100.0%	74	5.5%
c1908	258	645	33.8%	1782	93.4%	377	19.8%	385	466	24.4%	1412	74.0%	120	6.3%
c2670	701	1204	45.1%	2557	95.8%	278	10.4%	1109	734	27.5%	1839	68.9%	138	5.2%
c3540	831	1820	51.4%	3284	92.8%	505	14.3%	1137	1303	36.8%	3034	85.7%	227	6.4%
c5315	1134	1917	36.1%	5199	97.8%	620	11.7%	1867	1452	27.3%	4149	78.1%	405	7.6%
c6288	172	5447	86.6%	6288	100.0%	5602	89.1%	210	3028	48.2%	6288	100.0%	825	13.1%
c7552	1037	3186	42.2%	6946	92.0%	2046	27.1%	1743	2564	34.0%	5398	71.5%	500	6.6%
Average	498	1566	49.4%	2908	95.4%	981	22.3%	766	1067	34.9%	2495	83.0%	242	7.4%

* Fault efficiency=100%

that a present tracing gate during the backward/ propagation operation is Gp. Let {G1, G2, ..., Gn} be a set of gates feeding/connecting to the gate Gp. Lv(G) denotes the level of a gate G (i.e., the maximum number of stages from PI to G (from G to PO for the propagation operation)), and In(G) denotes the number of input lines of G that we must assign logical values for the backward/propagation operation. We select a gate to minimize the value S(Gi) of the following equation.

$$S(Gi) = \frac{In(Gi)}{Lv(Gp) - Lv(Gi)}, (1 \le i \le n) \quad (6)$$

By using the equation, we can select a path that can minimize locally the number of lines with specified logical values. The column "Proposed" shows ATPG results by the proposed method (modified PODEM algorithm). Although the number of test vectors increases by approximately 46% than that of the original PODEM on the average, the number of lines with *don't care* increases by approximately 29%. Therefore, we can stabilize the wire capacitances around the fault location if we use the test vectors generated by the proposed method.

Even if we use the above test vectors, signal values around the fault location will change after a test vector is applied. In this situation, we can consider the following condition for applying a test vector at time t3 (see Fig 2).

Cw1 ← Cw1+/-ΔCw, Cw2 ← Cw2-/+ΔCw

Note that the total wire capacitance, Cw1+Cw2, around any signal line never changes because circuit design does not change (Cw1+Cw2=constant).

When a test vector is applied and voltages of signal lines around a fault location change, the faulty circuit behaves like a step-voltage application. According to Eq. (2), the voltage at the fault location is in proportion to Cw1/(Cw1+Cw2) mainly. Therefore, the voltage at the fault location becomes higher (lower) for the VDD application as Cw1 (Cw2) is larger, and as a result, the delay time caused by the fault becomes shorter (longer) compared with unchanged wire capacitances. We can obtain the opposite relationship for the VSS application. Table 4 shows simulation results when wire capacitances change at time t3 (the time when a test vector is applied). As described in Sect. 2, the VDD (VSS) application is better for Cw1<Cw2 (Cw1>Cw2) (indicated by * in Table 4). However, if the wire capacitances change when the test vector is applied, and the delay time decrease, then the other test type is appropriate for such a case. For example, the VDD application is better for (Cw1, Cw2)=(8fF, 80fF) because of the lower Vfmax and the longer tpd. If (Cw1, Cw2) changes to (80fF, 8fF) for applying the test vector, the delay time becomes shorter from 6.72μsec to 0.022μsec. In this case, the VSS application is better because the final values of wire capacitances after the test vector application are (80fF, 8fF). From the above discussion, two methods of the voltage application, VDD application and VSS application, give good results even if the wire capacitances around the fault location change.

Table 4 Results of change in wire capacitances.

Sim. No.	Test & Circuit types	Cw1 [fF]	Cw2 [fF]	Vfmax [mV]	tpd [μs]	
S6	Typical gates	80	8	698.9	6.76	
		80 → 44	8 → 44	698.9	9.38	
		80 → 8	8 → 80	698.9	12.45	
S7	VDD application	8	80	127.1	6.72	*
		8 → 44	80 → 44	127.1	2.67	
		8 → 80	80 → 8	127.1	0.022	
S8	Typical gates	80	8	-102.0	6.65	*
		80 → 44	8 → 44	-102.0	2.54	
		80 → 8	8 → 80	-102.0	0.023	
S9	VSS application	8	80	-675.7	6.65	
		8 → 44	80 → 44	-675.7	9.88	
		8 → 80	80 → 8	-675.7	11.79	

4. Conclusions

We showed the ability of our testing method for interconnect open faults. Since the behavior of the faulty circuit can be modeled by the RC differential circuit if we use the proposed method, we can estimate electrical behaviors by using a simple and a local circuitry around a fault location. Moreover, this paper exposed that the method can apply to open faults with any value. Finally, we showed test generation results that are suitable for the proposed testing method and are achieved by the ATPG algorithm similar with stuck-at faults. In order to show practicality, we further apply the proposed method to a real chip and examine it for other open fault models.

References

[1] J. Figueras, "Test Challenges in Nanometric World," Invited Talk, 2nd IEEE Latin American Test Workshop, 2001.

[2] R. Rodríguez-Montañés, P. Volf, and J. Pineda de Gyvez, "Resistance Characterization for Weak Open Defects," IEEE Design & Test Computers, vol.19, no.5, pp.18-26, 2002.

[3] J. Segura, A. Keshavarzi, J. Soden, and C. Hawkins, "Parametric Failures in CMOS ICs – A Defect-Based Analysis," Proc. Int. Test Conf., pp.90-99, 2002.

[4] V.H. Champac and A. Zenteno, "Detectability Conditions for Interconnection Open Defect," Proc. VLSI Test Symp., pp.305-311, 2000.

[5] B. Kruseman, "Comparison of Defect Detection Capabilities of Current-based and Voltage-based Test Methods," Proc. European Test Workshop, pp.175-180, 2000.

[6] J.C.-M. Li, C.-W. Tseng, and E.J. McCluskey, "Testing for Resistive Opens and Stuck Opens," Proc. Int. Test Conf., pp.1049-1058, 2001.

[7] C.-W. Tseng and E.J. McCluskey, "Multiple-Output Propagation Transition Fault Test," Proc. Int. Test Conf., pp.358-366, 2001.

[8] S. Ghosh and F.J. Ferguson, "Estimating Detection Probability of Interconnect Opens using Stuck-at Tests," Proc. Great Lakes Symp. VLSI, pp.254-259, 2004.

[9] Y. Miura, "Open Fault Detection in CMOS Combinational Circuits by Logic Testing with Precharge," Information Technology Letters, Forum on Information Technology, LC-005, pp.39-42, 2004.

[10] J.M. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice-Hall, NJ, 1996.

[11] Z. Li, X. Lu, W. Qiu, W. Shi, and D.M.H. Walker, "A Circuit Level Fault Model for Resistive Opens and Bridges," Proc. VLSI Test Symp., pp.379-384, 2003.

[12] The MOSIS Service, http://www.mosis.org/.