7T-1

Deadlock avoidance in construction of n FSM's

Yao-Xue Zhang, Norio Shiratori, and Shoichi Noguchi

Research Institute of Electrical Communication, Tohoku University

1. Introduction

Communication systems and their protocols can be modeled in n Finite State Machines (FSM's) which exchange messages over m FIFO, error-free and unidirectional channels. In construction of these FSM's, a designer may easily fall in creating some logical errors, such as *deadlocks* which imply that at least two FSM's are waiting each other to receive messages, but no message is sent to them. This paper proposes some design rules to protect a designer from creating deadlocks.

2. Preliminary

Let $\{P_1, P_2, ..., P_i, ..., P_n\}$ be n FSM's. Let $\{C(1,2), C(1,3), ..., C(i,j), ...\}$ $(i \neq j)$ be m channels connecting n FSM's. Where, C(i,j) is a channel over which FSM P_i sends messages to FSM P_j. Let S be a global state which consists of current state (or node) of each P_i $(1 \leqq i \leqq n)$, and current message sequence in each C(i,j) $(1 \leqq i, j \leqq m$ and $i \neq j)$. An initial global state is one where the state element of each FSM is an initial one and the message sequence element of each channel is empty. We assume that a designer constructs n FSM's by first constructing the global state transition graph from the given initial global state. Moreover, we assume that the message transmissions are instantaneous.

Definition 1 *Communicatable*

We define that two FSM's P_i and P_j $(1 \leqq i, j \leqq n$ and $i \neq j)$ are communicatable,

iff,

$\exists_{i,j\,(1 \leqq i, j \leqq m \text{ and } i \neq j)}$ C(i,j) and C(j,i) exist.□

Definition 2 *History reception vector*

We define a history reception vector $H_i = <h_i^1, h_i^2, ..., h_i^k, ..., h_i^y>$ for each FSM P_i $(1 \leqq i \leqq n)$.

Where,

y is the number of produced states of P_i,

h_i^k is a twin state,

$h_i^k = <q_i^k, <ch_{lir}^k>_{1 \leq l \leq m, 1 \leq r \leq x}>$, and

q_i^k: a state (node) of FSM P_i,

ch_{lir}^k: a received message sequence from channel C(l,i) which constructs path r of P_i whose origin is q_i^k and whose termination is a state where no transmission has occurred, x is the number of paths whose origins are q_i^k. □

Definition 3 *Input function*

Let FSM's P_i and P_j $(i \neq j)$ be communicatable. We define an input function $Input_i(P_j,t) = e$ for P_i and P_j. Where, e is the number of messages in the channel C(i,j) at time t. □

3. Deadlock avoidance rules

Underlying the definitions given in Section 2, we give the following rules to help protocol designers to decide the entry states of message transmissions or receptions. Here, we let the current global state be S^k from which the transitions occur. Also, let FSM's P_i and P_j be communicatable and a message transmission have been specified (by a designer) at state q_i^k of P_i included in S^k or a reception have occurred at q_i^k. Other FSM's have the same characteristics.

Rule 1

<u>If</u> for $\forall_{r(1 \leqq r \leqq x)}$ $Input_i(P_j,t) \geqq |ch_{ijr}^k|$, where, ch_{ijr}^k belongs to h_j^k and $|ch_{ijr}^k|$ is the number of messages in sequence ch_{ijr}^k;

<u>then</u> a designer can select any produced state of process P_i or assign a new state as the entry state of occurred transmission or reception;

<u>else if</u> $\exists_{r(1 \leqq r \leqq x)}$ $Input_i(P_j,t) < |ch_{ijr}^k|$;

then compare the message sequence in C(i,j) with ch_{ijr}^k,

if the message sequence in C(i,j) is a prefix of ch_{ijr}^k,

then check the history vector H_i and the input function $Input_j(P_i,t)$,

else the designer can select any produced state of process P_i or assign a new state as the entry state of occurred transmission or reception.

Check the history vector H_i and the input function $Input_j(P_i,t)$:

If for $\forall r(1 \leqq r \leqq x')$ $Input_j(P_i,t) \geqq |ch_{jir}^k| - \delta$, where ch_{jir}^k belongs to h_i^k, $\delta = 1$ if a reception has occurred at q_i^k, otherwise, $\delta = 0$;

then the designer can select any produced state of process P_i or assign a new state as the entry state of occurred transmission or reception;

else if $\exists r(1 \leqq r \leqq x')$ $Input_j(P_i,t) < |ch_{jir}^k|$;

then compare the message sequence in C(j,i) with those ch_{jir}^l ($1 \leqq l \leqq y$, y is the number of produced states of FSM Pi until time t) belonging to h_i^l,

if the message sequence in C(j,i) is not a prefix of ch_{jir}^l,

then q_i^l is a candidate of the entry state,

else if $Input_j(P_i,t) \geqq |ch_{jir}^l|$,

then q_i^l is a candidate of the entry state,

else q_i^l can not be assigned as the entry state. □

Rule 2

If there does not exist a produced state q_i^l which can be selected as a candidate of the entry state of an occurred transmission or reception by above Rule 1;

then the designer assigns a new state as the entry state. □

Rule 3

If a) $\exists r(1 \leqq r \leqq x)$ $Input_i(P_j,t) \geqq |ch_{ijr}^k|$,

b) the message sequence in C(i,j) is a prefix of ch_{ijr}^k,

c) channel C(j,i) is empty and q_i^k is a new state where the message transmission can be specified;

then require the designer to specify transmissions at q_i^k. □

4. Conclusions

We have proposed some design rules to help designers to construct n FSM's without logical error deadlocks in this paper. It is useful to utilize these rules to construct communication protocols represented in FSM's.

References:

[1] D.Brand and P.Zafiropulo," On communicating finite state machines," JCAM, vol.30, No.2, pp.323-342, Apr. 1983.

[2] Y-X. Zhang, K.Takahashi, N. Shiratori and S. Noguchi, "An interactive protocol synthesis algorithm using a global state transition graph," IEEE Trans. Software Eng., vol.14, No.3, pp.394-404, March 1988.